


LCFC Confidential

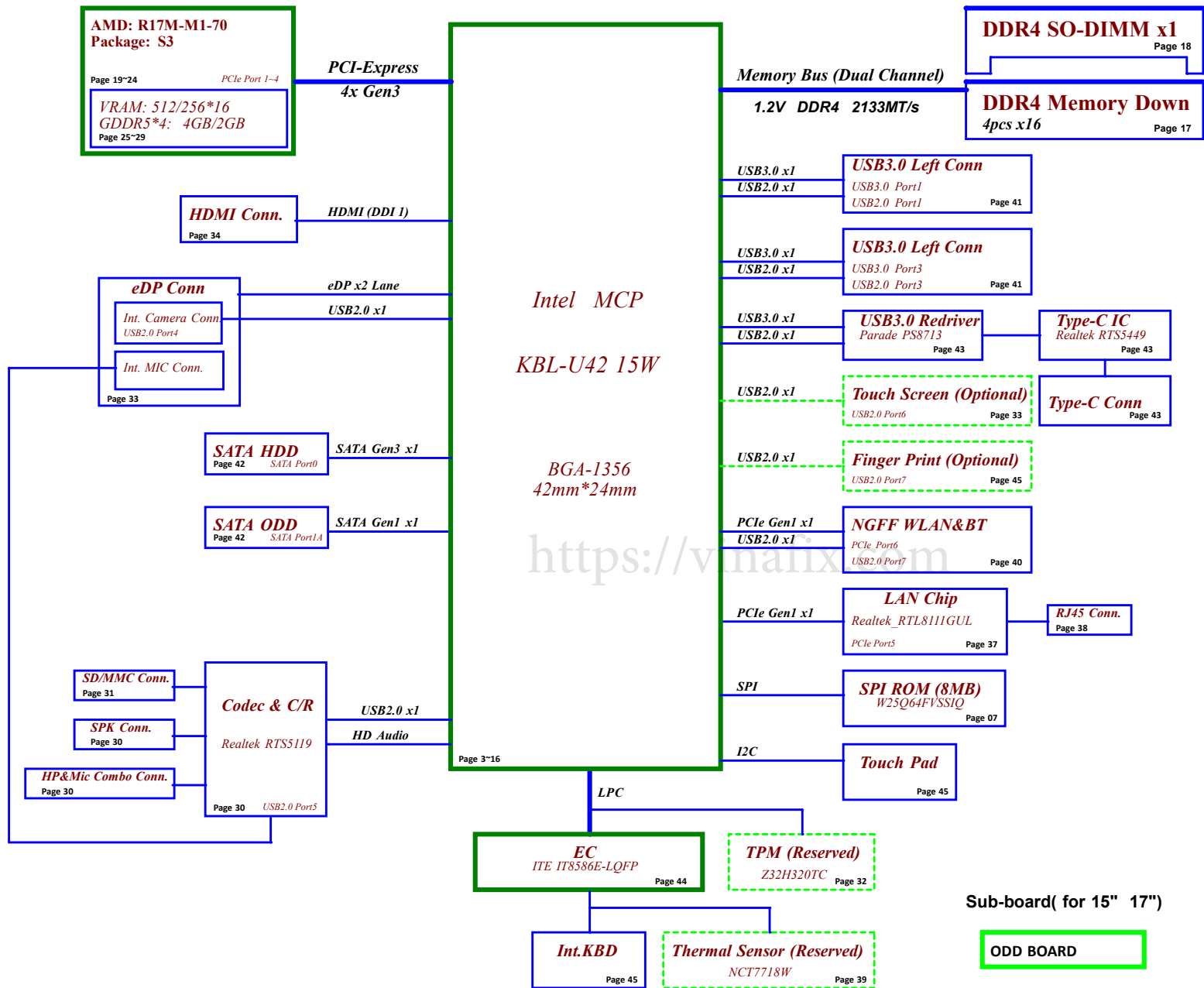
EG523 MB Schematics Document

Kabylake-U42 with DDR4 + AMD R17M-M1-70 GPU with GDDR5

2017-03-15

<http://vinafix.com>
REV: 0.1

Security Classification		LC Future Center Secret Data		Title					
Issued Date		2016/12/14		Deciphered Date		2017/12/13			
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Voltage Rails (0 --> Means ON , X --> Means OFF)

Power Plane				
State	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.0VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	0	0	0	0
S3	0	0	0	X
S3 Battery only	0	0	0	X
S5 S4 AC Only	0	0	X	X
S5 S4 Battery only	0	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	V +3VG_AON	V +3VS	X	V +3VALW_PCH	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	V +3VS

EC SMBus1 address EC SMBus2 address EC SMBus3 address PCH SM Bus address

Device	Address	Device	Address	Device	Address	Device	Address
Smart Battery	need to update	Thermal Sensor(NCT7718W)	1001_100xb	DDR4 SODIMM	need to update	Wlan	need to update
Charger	0001 0010 b	PCH	need to update				
		DGPU	need to update				

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

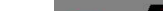
HSIO PORT		Function
USB3.0	1	USB3.0 Conn Left
	2	USB Type-C
	3	USB3.0 Conn Left
	4	NC
	5	NC
	6	NC
USB2.0	1	USB3.0 Conn Left
	2	USB Type-C
	3	USB3.0 Conn Left
	4	Finger Print
	5	Cardreader
	6	Touch Panel
	7	Bluetooth
	8	Camera
	9	NC
	10	NC
PCIE	1~4 X4 PCIE	DGPU
	5	LAN
	6	WLAN
	7	SATA HDD
	8	SATA ODD
	9~12 X4 PCIE	Optane Memory
SATA	0	HDD
	1A	ODD
	1B	used as PCIE
	2	used as PCIE

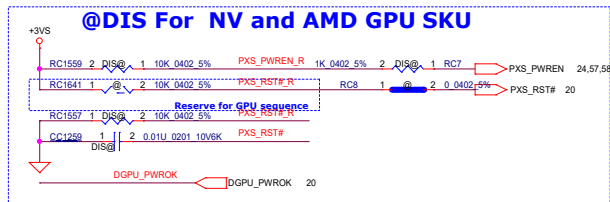
BOM Structure	BTO Item
@	Not stuff
14@	For 14" part
15@	For 15" part
14or15@	For 14" or 15" part
14or17@	For 14" or 17" part
Cannonlake@	For Cannonlake part
CD@	For C cost down
DUALMIC@	For Dual MIC part
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC nu-stuff part
EMC_PX@	For EMC PX part
EMC_PXNS@	For EMC PX nu-stuff part
ES@	For ES CPU
EXO@	For EXO GPU
ME@	For ME part
NTS@	For nu-touch part
DIS@	For GPU part
OPT@	For NV GPU part
PX@	For AMD GPU part
RANKA@	For VRAM rank A part
RANKB@	For VRAM rank B part
Realtek SD@	For Realtek SD part
SINGLEMIC@	For single MIC part
SINGLERANK@	For single VRAN rank part
DUALRANK@	For dual VRAN rank part
TS@	For touch screen part
TPM@	For TPM part
UMA@	For UMA part



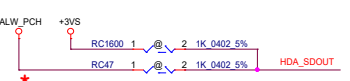
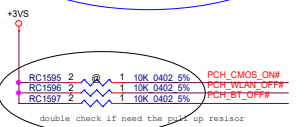
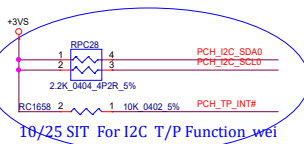
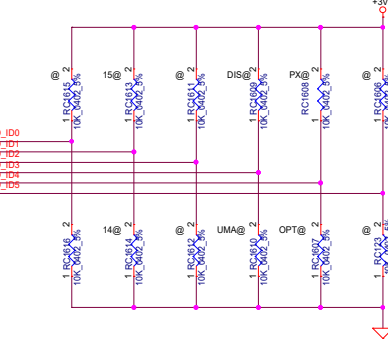
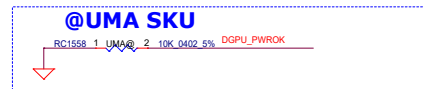
check DDPC_CLK pull high or not?

Disable DDI2 G320 SDV wei

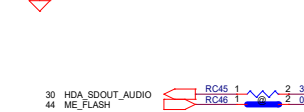
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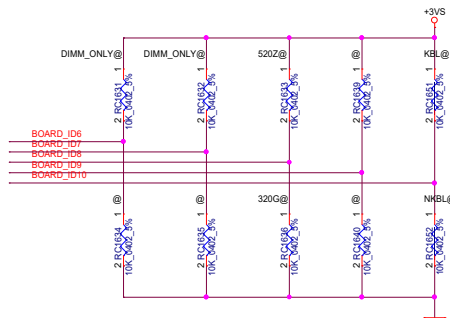
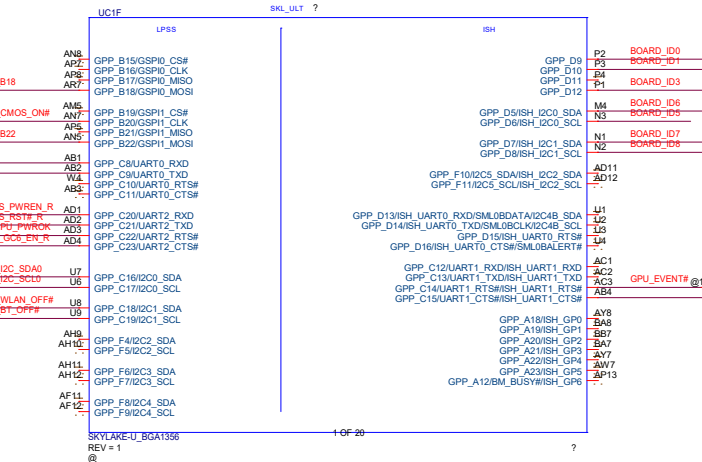
@OPT&GC6 Only for NV GPU SKU



0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security(override). This strap should only be asserted high during external pull-up in manufacturing/debug environments ONLY.



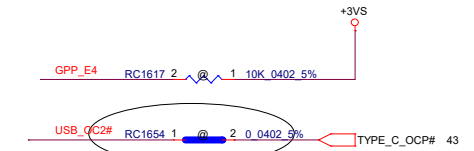
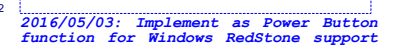
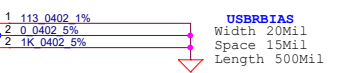
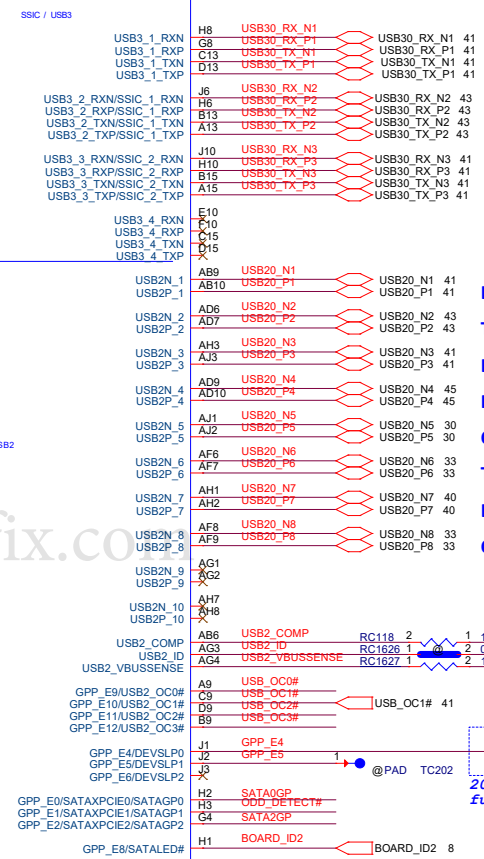
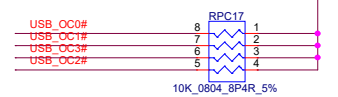
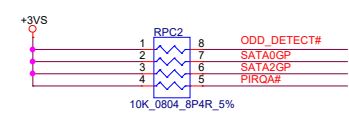
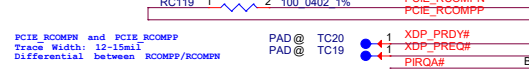
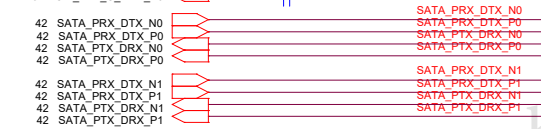
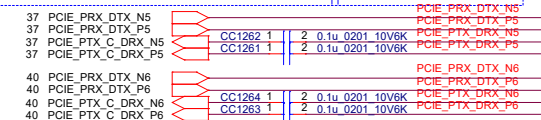
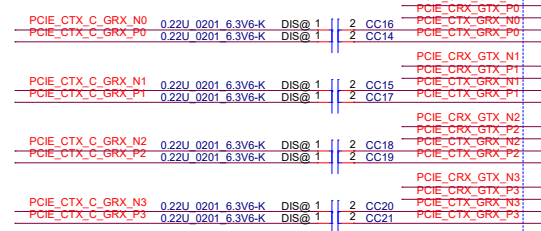
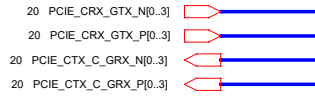
Pin Name	Strap Description	Configuration	Default Value	When Sampled
SPKR / GPP_B14	Top Swap Override	Internal PD 0 = Disable " Top Swap" mode. (Default) ★ 1 = Enable " Top Swap" mode	0	Rising edge of PCH_PWROK
GSPI0_MOSI /GPP_B18	No Reboot	Internal PD 0 = Disable " No Reboot" mode. (Default) ★ 1 = Enable " No Reboot" mode	0	Rising edge of PCH_PWROK
GSPI1_MOSI /GPP_B22	Boot BIOS Strap Bit BBS	Internal PD 0 = SPI (Default) ★ 1 = LPC	0	Rising edge of PCH_PWROK



Board ID	Description	Stuff R
Board ID [0:1]	00 14"	RC1616 RC1614
	01 15"	RC1616 RC1613
	10 17"	RC1615 RC1614
	11 Reserved	RC1615 RC1613
Board_ID2	0 Reserved	RC1612
	1 Reserved	RC1611
Board_ID3	0 UMA	RC1610
	1 DIS	RC1609
Board_ID4	0 NV GPU	RC1607
	1 AMD GPU	RC1608
Board_ID5	0 Reserved	RC1623
	1 Reserved	RC1606


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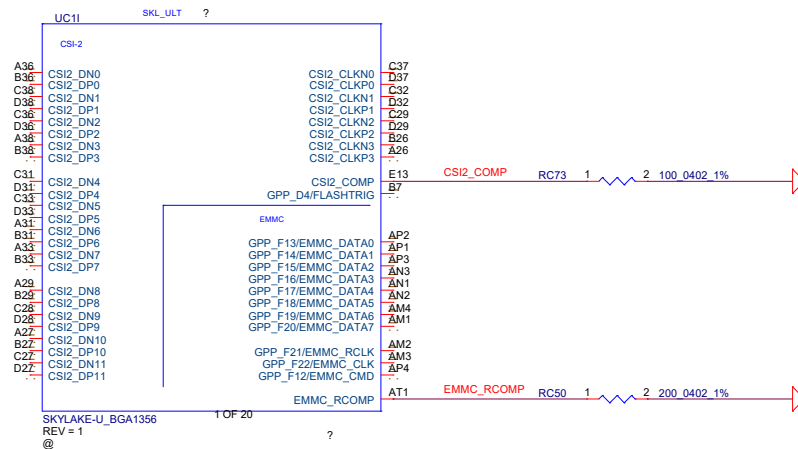
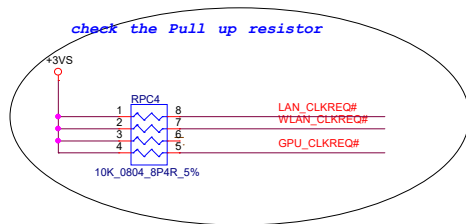
@DIS For NV and AMD GPU SKU



8/24 Reserve TYPE_C_OCP# to CPU USB_OC2# wei

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@DIS For NV and AMD GPU SKU

PCIE CLK0 DGPU

20 CLK_PCIE_GPU#
20 CLK_PCIE_GPU#
21 GPU_CLKREQ#

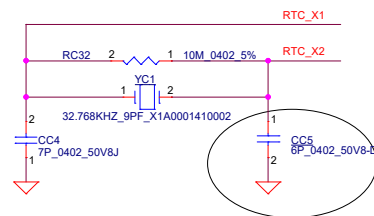
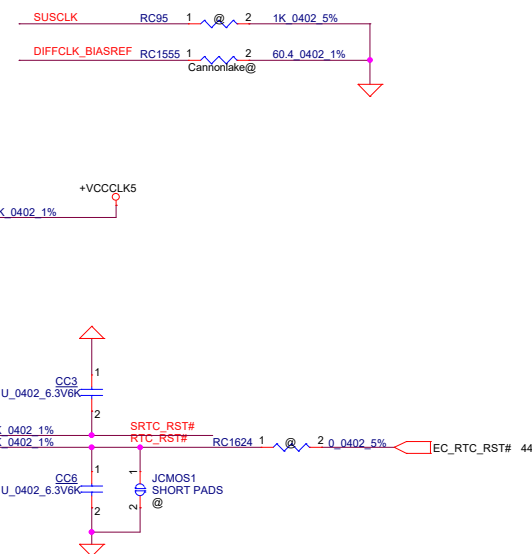
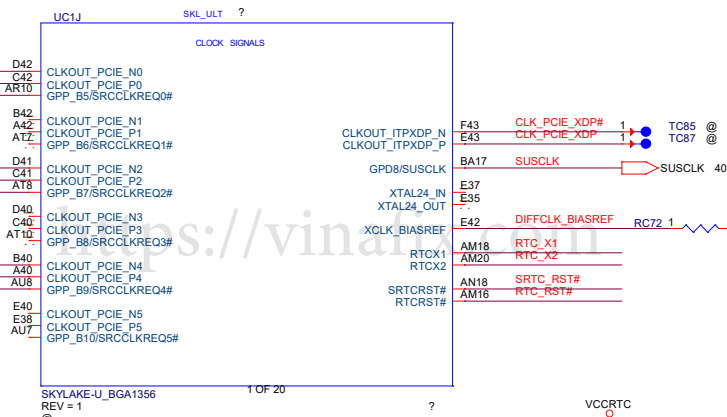
Optane memory

PCIE CLK5 WLAN

40 CLK_PCIE_WLAN#
40 CLK_PCIE_WLAN#
40 WLAN_CLKREQ#

PCIE CLK4 LAN

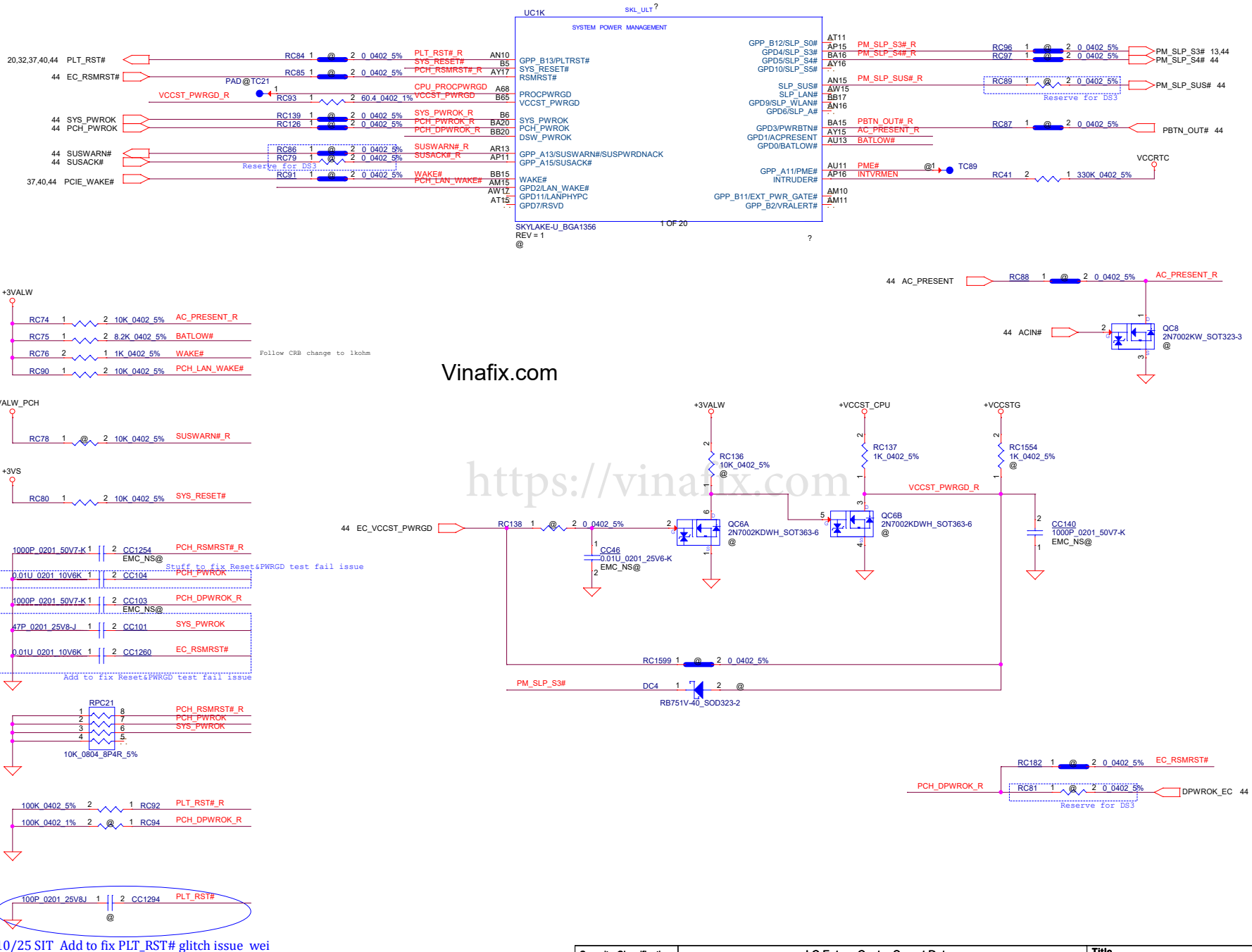
37 CLK_PCIE_LAN#
37 CLK_PCIE_LAN#
37 LAN_CLKREQ#



when single end external clock generator used, this pin should be grounded

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10/25 SIT Add to fix PLT_RST# glitch issue wei

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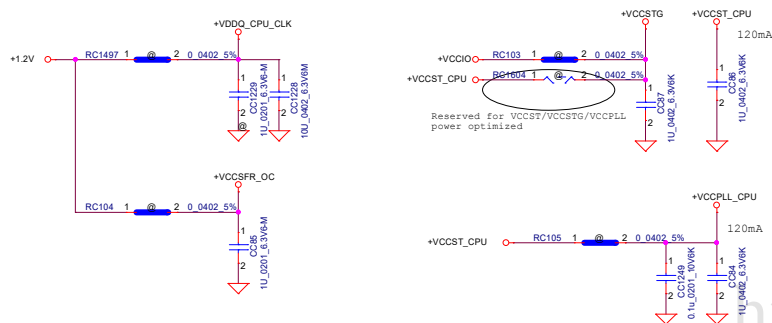
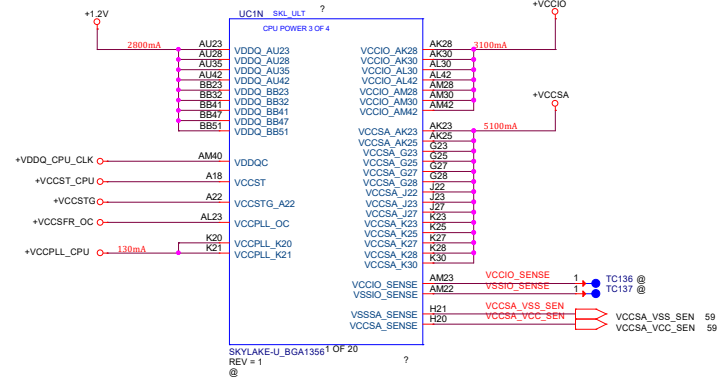
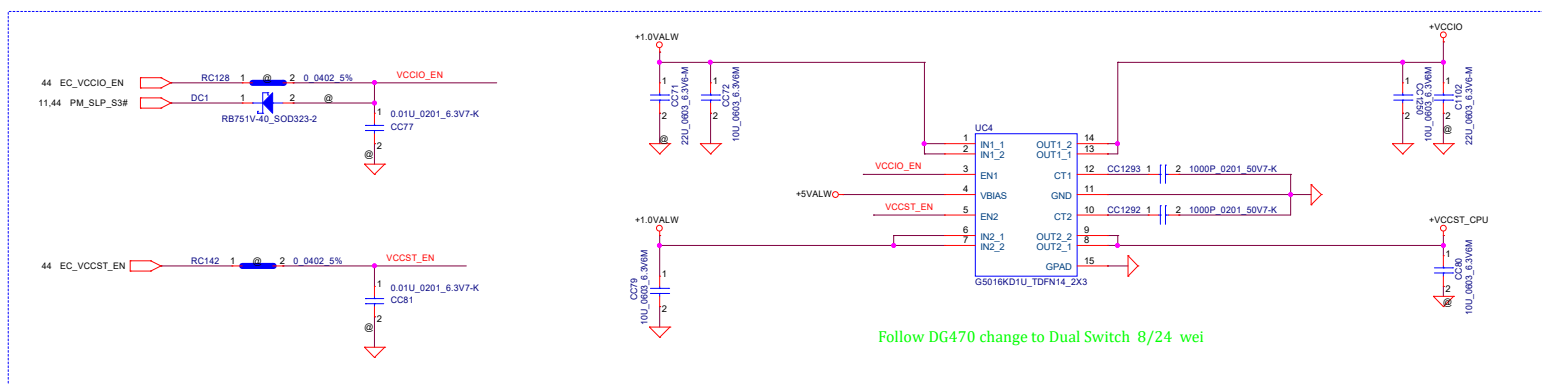

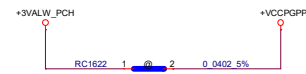


Figure 10 illustrates the schematic diagram of the VCCSA and VCCST power planes. The left side shows the VCCSA power plane, where the VCCSA_VCC_SEN signal is connected to RC101 (100 0402 1%) and the VCCSA_VSS_SEN signal is connected to RC102 (100 0402 1%). Both resistors are connected to the +VCCSA supply and ground. The right side shows the VCCST power plane, where the +1.0VALW signal is connected to RC1605 (100 0402 5%) and the +VCCST_CPU signal is connected to RC1605. Both resistors are connected to the +VCCST_CPU supply and ground. A note indicates that the circuit is reserved for VCCST/VCCSTG/VCCPLL power optimized.

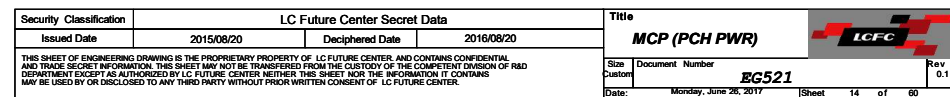


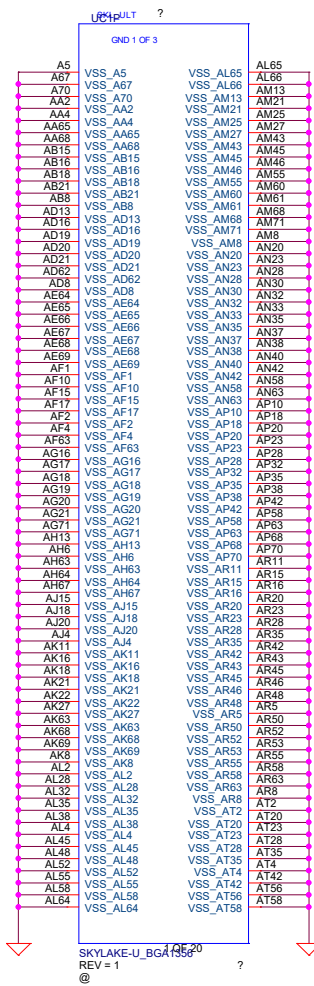
Follow DG470 change to Dual Switch 8/24 wei

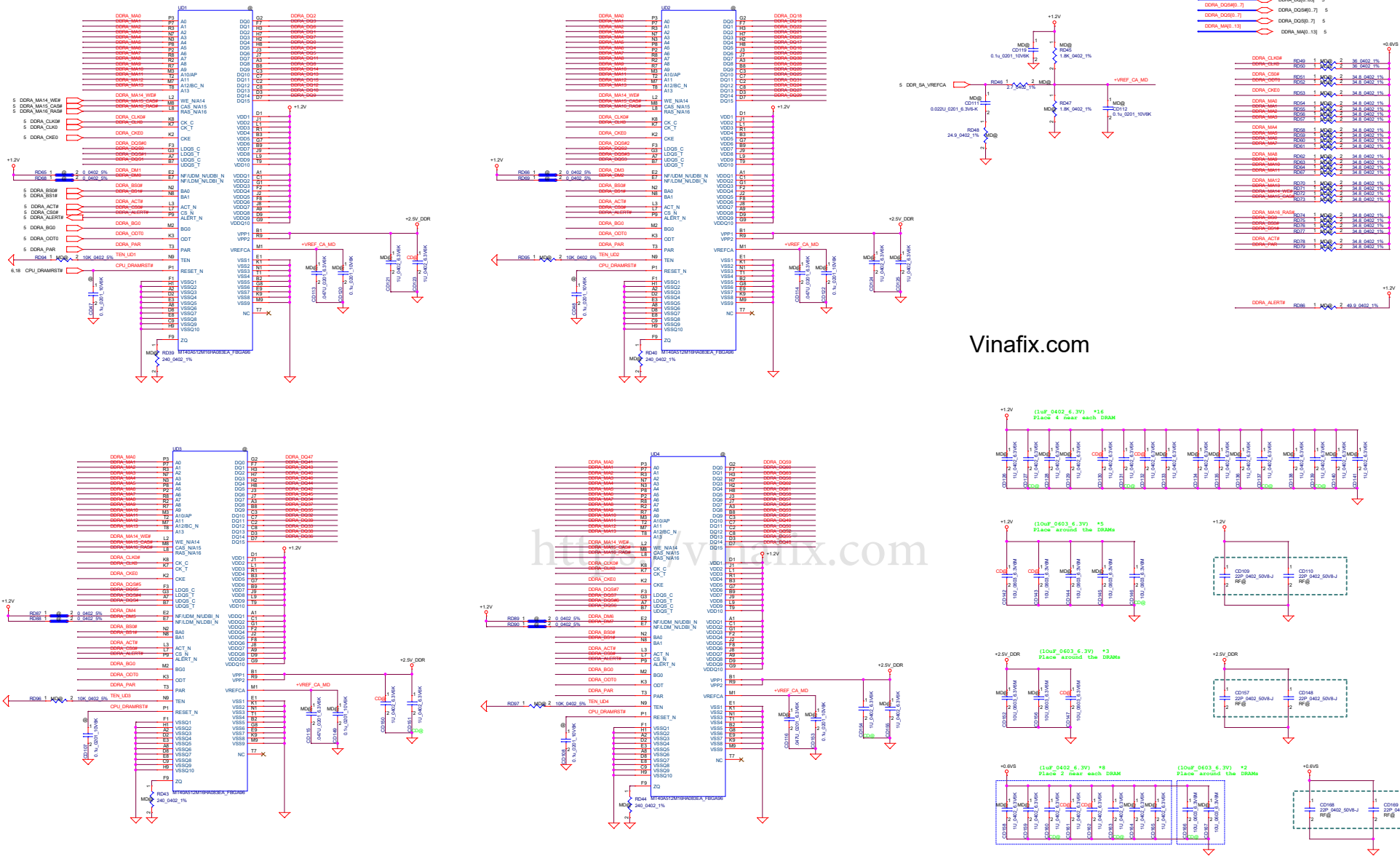
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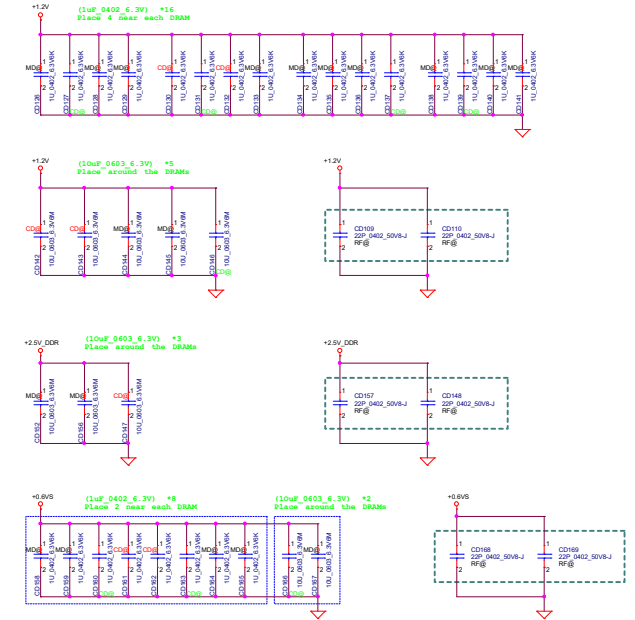
Pin	Signal	Current
V19	VCCAPLL_1P0	
AB17	VCCPRIM_1P0_AB17	
Y18	VCCPRIM_1P0_Y18	
AD17	VCCDSW_3P3_AD17	
AD18	VCCDSW_3P3_AD18	
K19	VCCCLK2	2.9mA
L21	VCCCLK3	2.4mA
N20	VCCCLK4	3.3mA



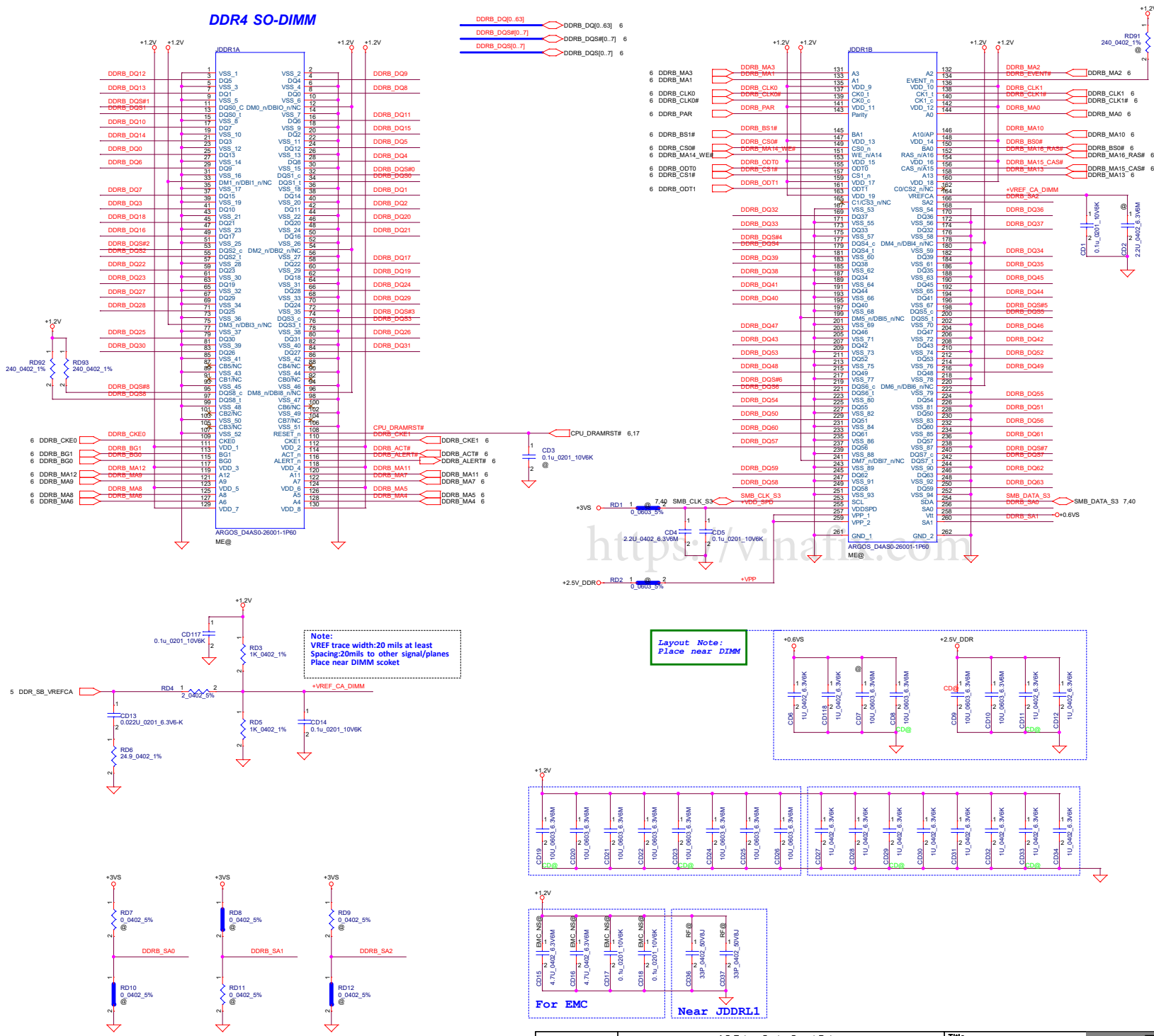





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DDR4 SO-DIMM



SPD Address = 2H

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Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μ s.

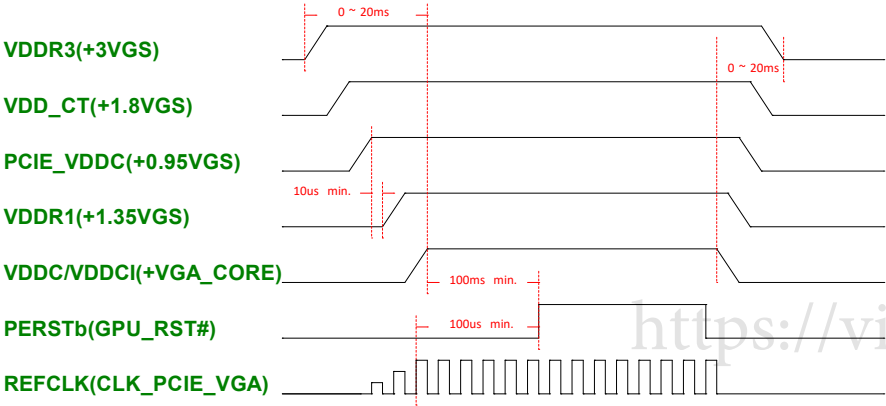
It is recommended that the 3.3-V rail ramp up first.

The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 μ s before VDDC, VDDCI, and VMEMIO start to ramp up.

The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU.

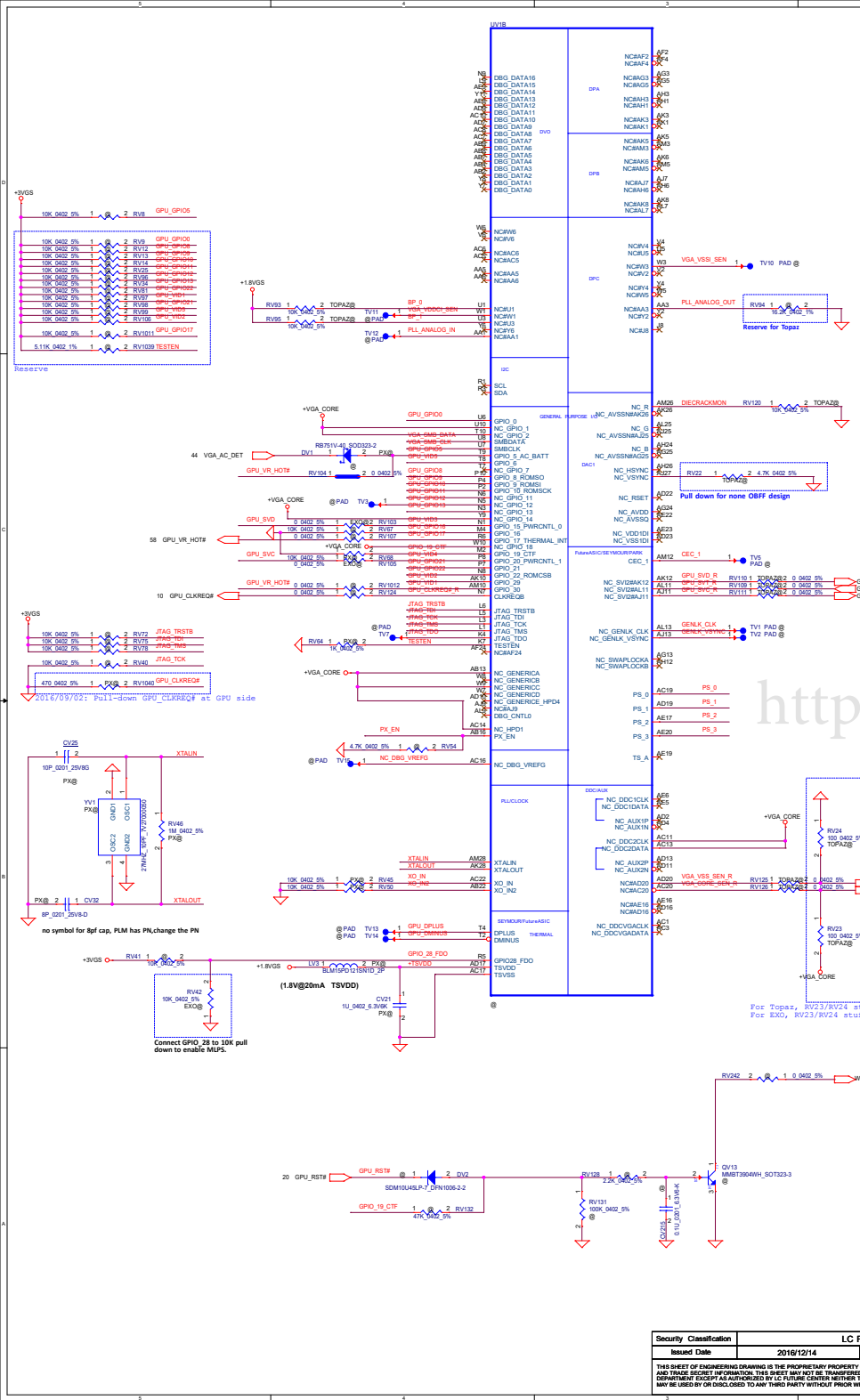
The gate circuits must meet the slew rate requirement (such as ≤ 50 mV/μ s)

For power down, reversing the ramp-up sequence is recommended.



VRAM ID config

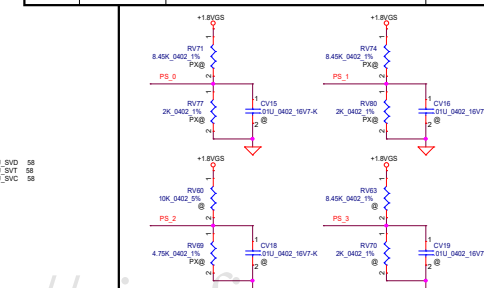
Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
4Gb GDDR5 256M x 16	Hynix H5GC4H24AJR-R0C 6.0Gbps@1.35V	100	4.53K	4.99K
	Micron EDW4032BABG-70-F 6.0Gbps@1.35V	111	4.75K	NC
	Samsung K4G41325FE-HC28 6.0Gbps@1.35V	110	3.4K	10K
8Gb GDDR5 512M x 16	Hynix H5GC8H24MJR-R0C 6.0Gbps@1.35V	000	NC	4.75K
	Micron MT51J256M32HF-70-A 6.0Gbps@1.35V	010	4.53K	2K
	Samsung K4G80325FB-HC28 6.0Gbps@1.35V	001	8.45K	2K



CONFIGURATION STRAPS

ALLOW FOR PULL-UP FOR THESE STRAPS AND IF THESE STRAPS ARE USED, THEY MUST NOT CONFLICT DURING RESET

MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[1]	ROM_CONFIG[0]	Define the ROM type when STRAP_BIOS_ROM_EN = 1	
PS_0[0]	ROM_CONFIG[1]	Define the primary memory aperture size when STRAP_BIOS_ROM_EN = 0	001 = 256MB
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	0 = PCIe GEN3 is supported. 1 = PCIe GEN3 is not supported.	1 = GEN3 is supported
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQ power management capability is disabled. 1 = The CLKREQ power management capability is enabled.	0
PS_1[3]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_1[4]	STRAP_TX_DRV_FULL_SWING	0 = The transmitter full-swing is enabled. 1 = The transmitter full-swing is disabled.	1
PS_1[5]	STRAP_TX_DEEMPH_EN	0 = 1x deemphasis disabled. 1 = 1x deemphasis enabled.	1 = Enable
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	0 = Disable
PS_2[4]	STRAP_BIF_VGA_DIS	0 = VGA controller capable enabled. 1 = The device will not be recognized as the system's VGA controller.	1
PS_2[5]	N/A	Reserved.	1
PS_3[1]	BOARD_CONFIG[0]	Board configuration related strap, such as for memory ID	
PS_3[2]	BOARD_CONFIG[1]	100 = Hynix 4Gb 110 = Micron 4Gb 111 = Samsung 4Gb	100 = Hynix 8Gb 110 = Micron 8Gb 001 = Samsung 8Gb
PS_3[3]	BOARD_CONFIG[2]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and used (Combine with PS_0[5]).	
PS_3[4]	AUD_PORT_CONN_PINSTRAP[1]	111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	11

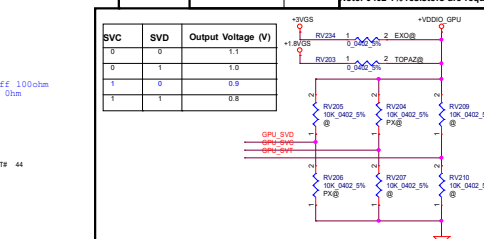


MLPS	5	4	3	2	1	BCM
PS_0[5:1]	1	1	0	0	1	RV71=8.45K RV77=2K CV15=NC
PS_1[5:1]	1	1	0	0	1	RV74=8.45K RV80=2K CV16=NC
PS_2[5:1]	1	1	0	0	0	RV60=NC RV69=4.75K CV18=NC
PS_3[5:1]	1	1	X	X	X	RV63=X76 RV70=X76 CV19=NC

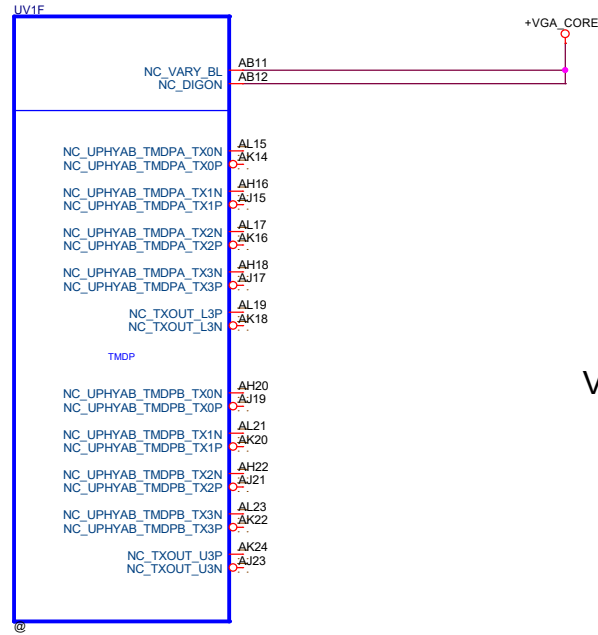
with BCM structure control, RV63, RV70 change to different value to adjust VRAM config with BCM structure control, when config PS63, RV74 change to 8.45K, RV80 change to 2K

Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

Note: 0402 1% resistors are required



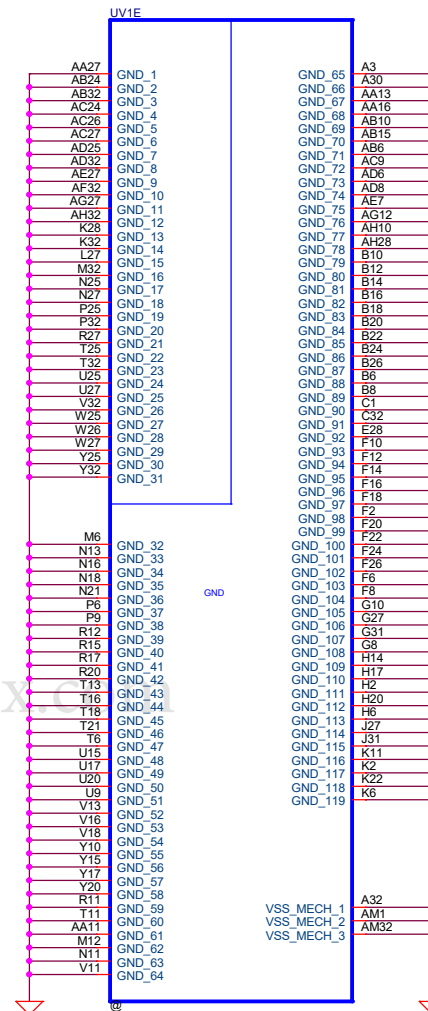
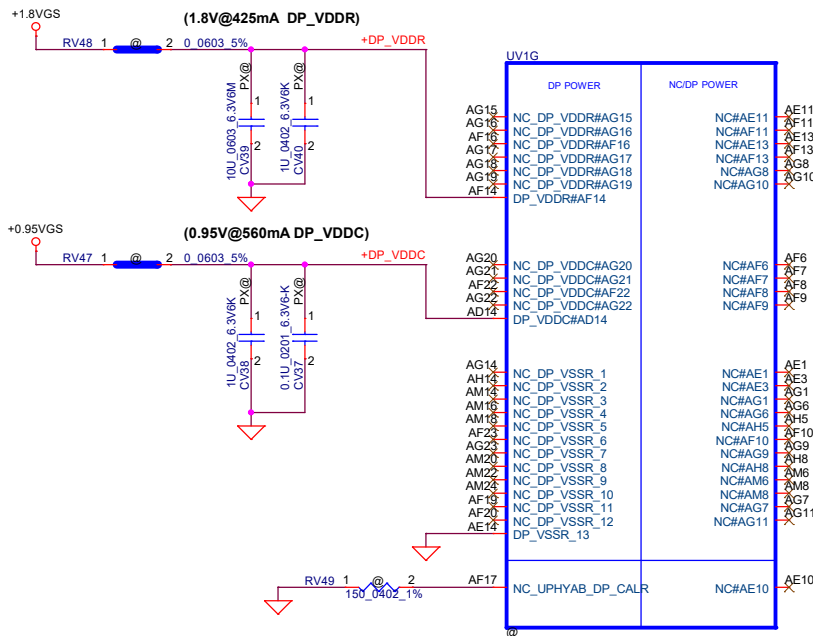
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Issued Date	2016/12/14	Deciphered Date	2017/12/13
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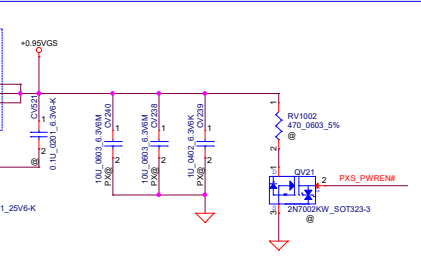
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Issued Date	2016/12/14	Deciphered Date	2017/12/13	ATI_R17M-M1-70_TMDP	
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				Date: Monday, June 26, 2017	Rev 0.1
				Sheet 22	of 60



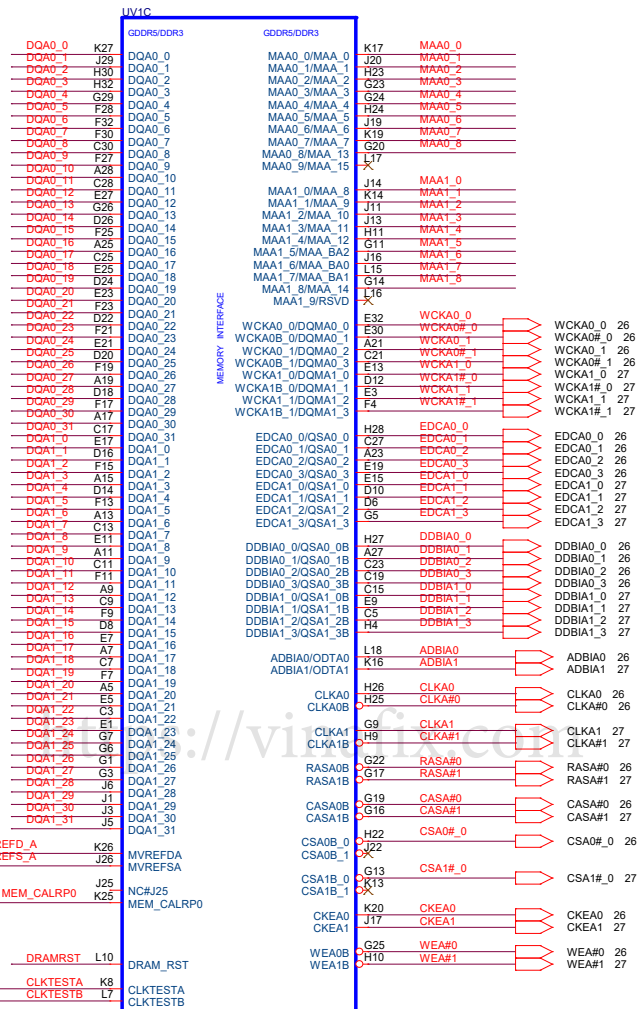
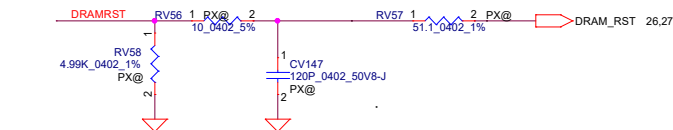
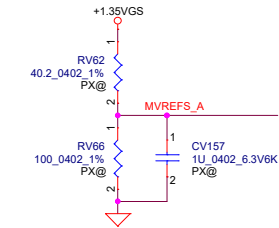
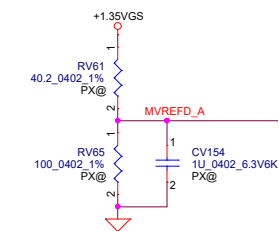
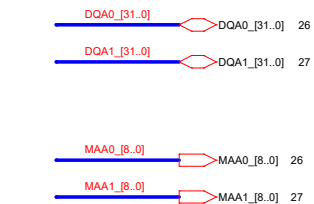
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				Sheet 25	of 60

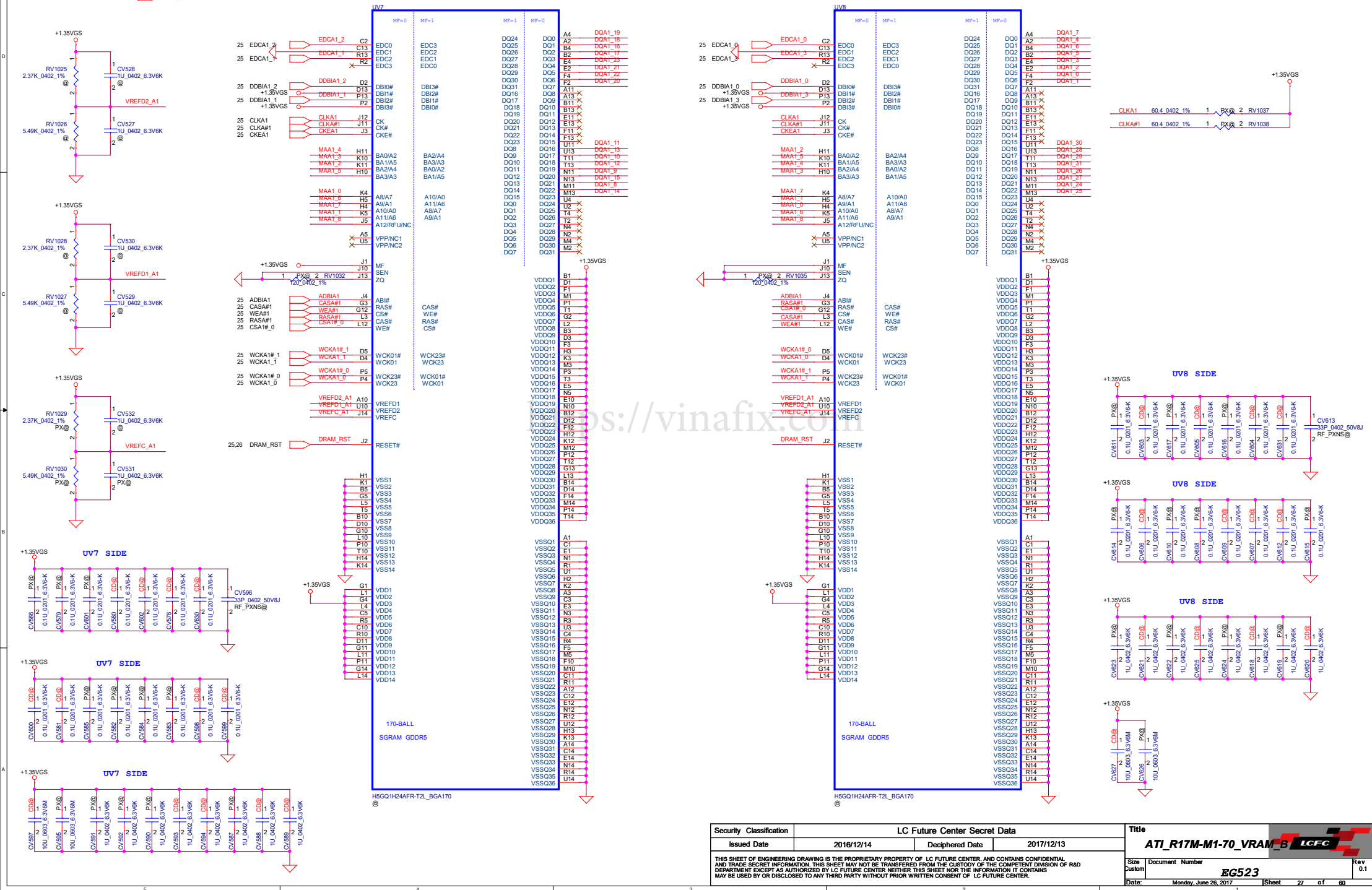
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Issued Date		2016/12/14	Deciphered Date		2017/12/13		ATI_R17M-M1-70_VRAM_A	
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Upper 32 bits

DQA1_[31..0] 25
MAA1_[8..0] 25


MF=1 Mirror

MF=0 No Mirror




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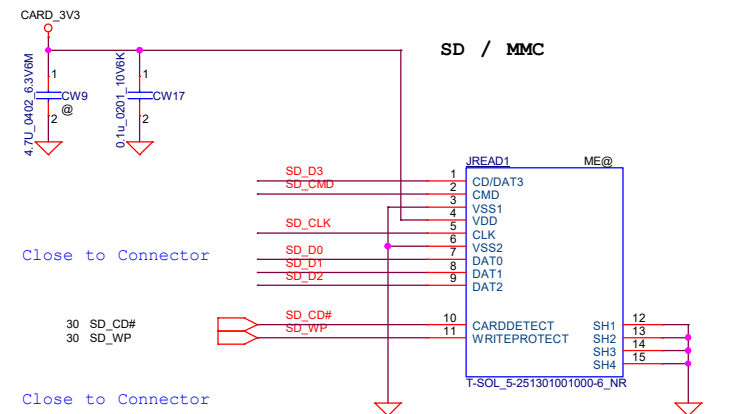
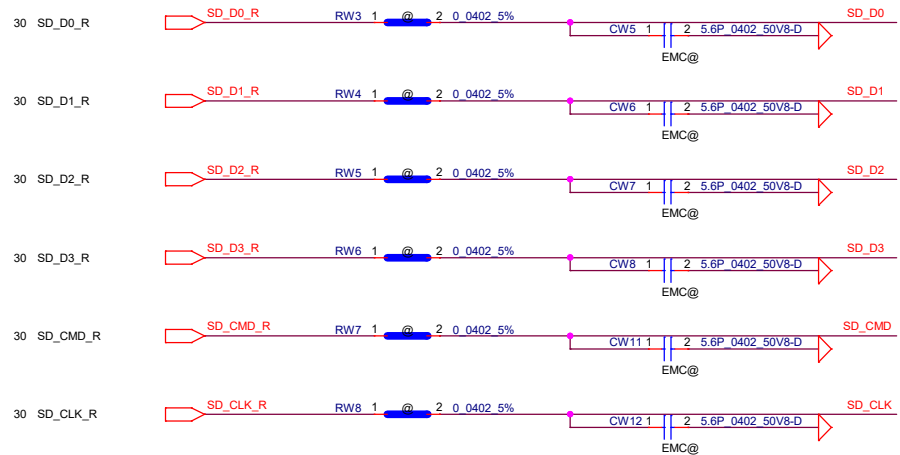
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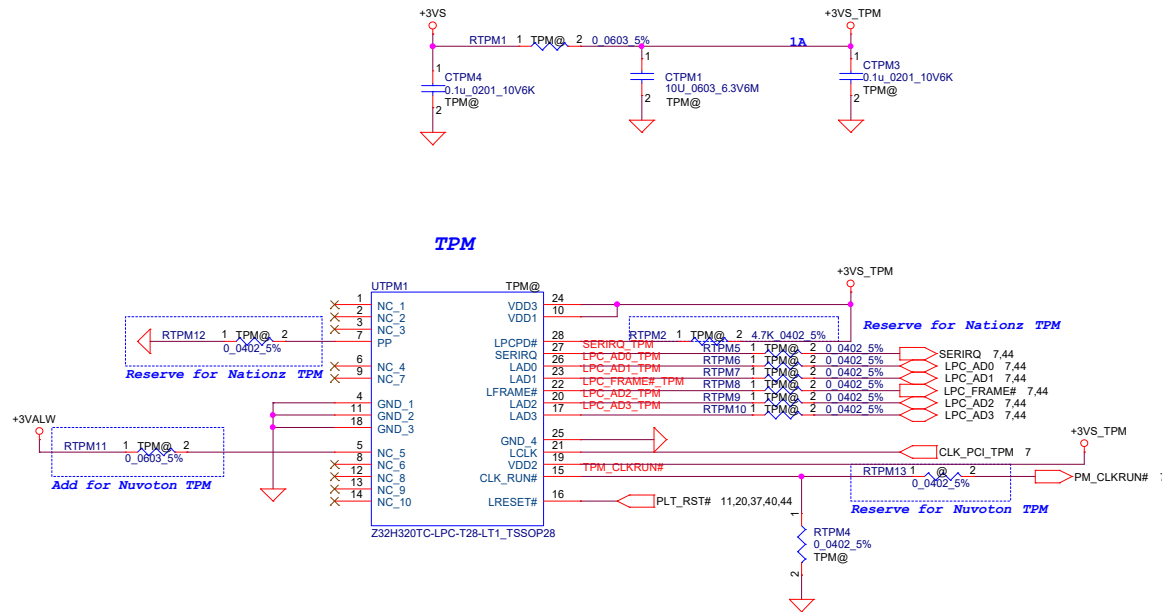
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8/16 Update Conn. P/N SP07000WG00 wei

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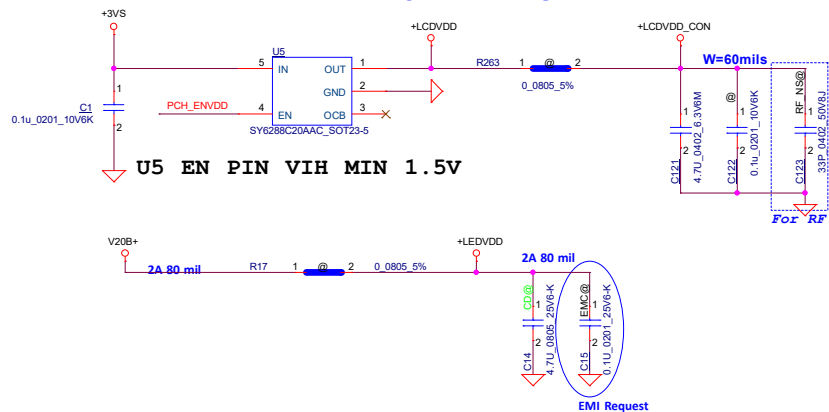
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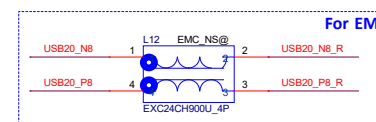
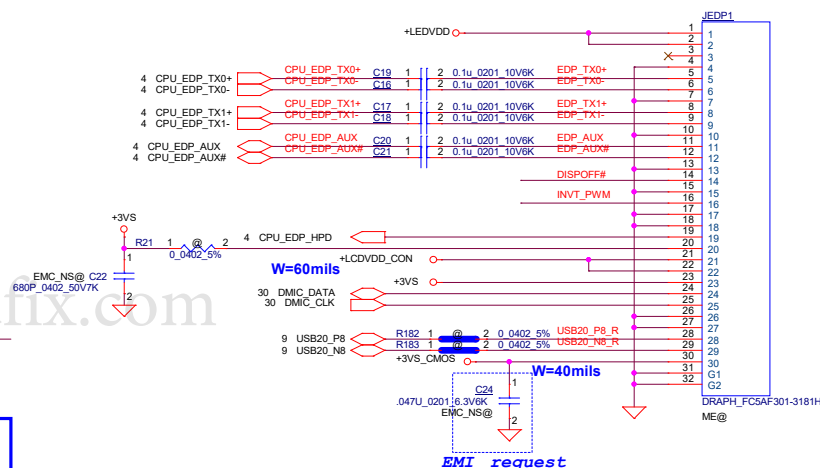
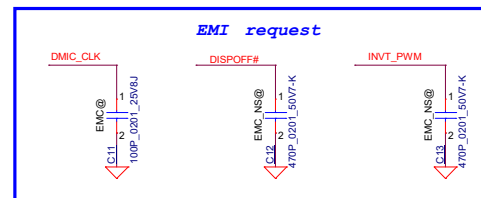
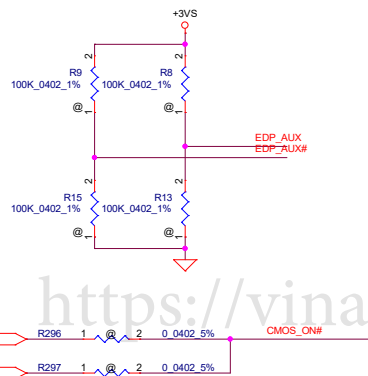
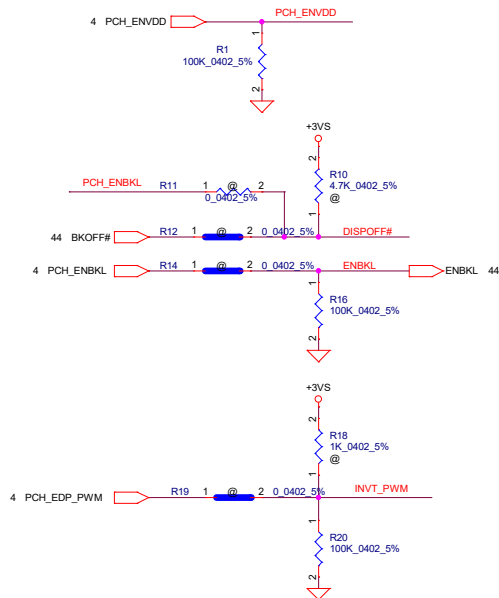
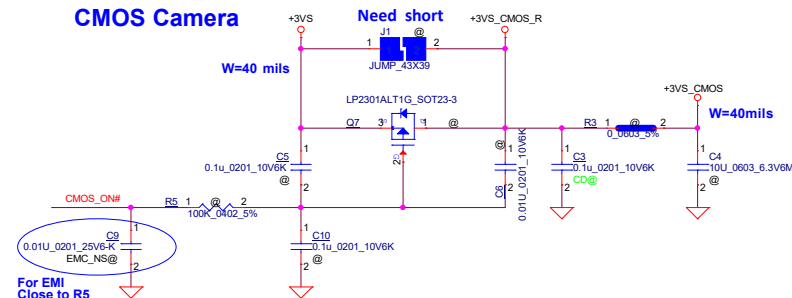
	Nationz TPM	Nuvoton TPM
RTPM2	Stuff	NC
RTPM12	Stuff	NC
RTPM11	NC	Stuff

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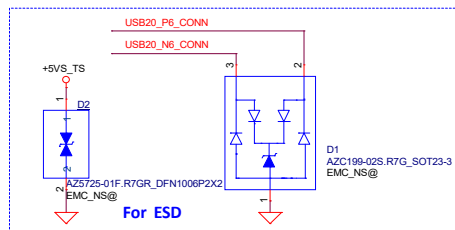
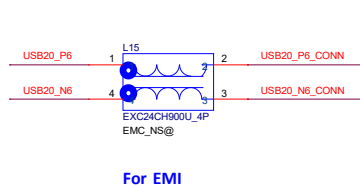
LCD POWER CIRCUIT



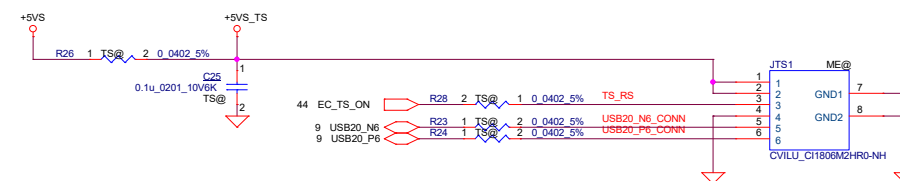
CMOS Camera



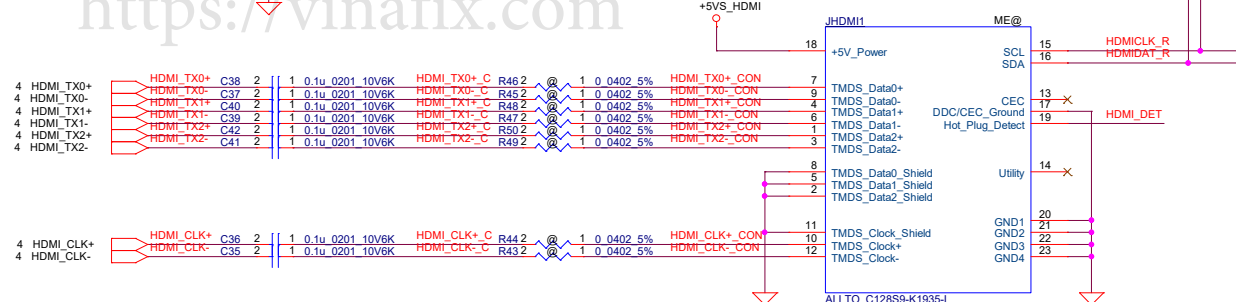
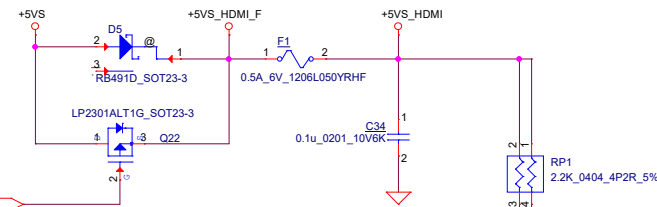
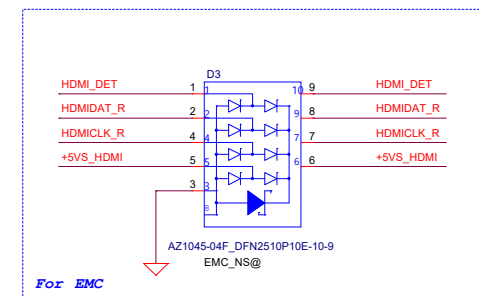
Touch Screen



Touch Screen

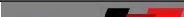


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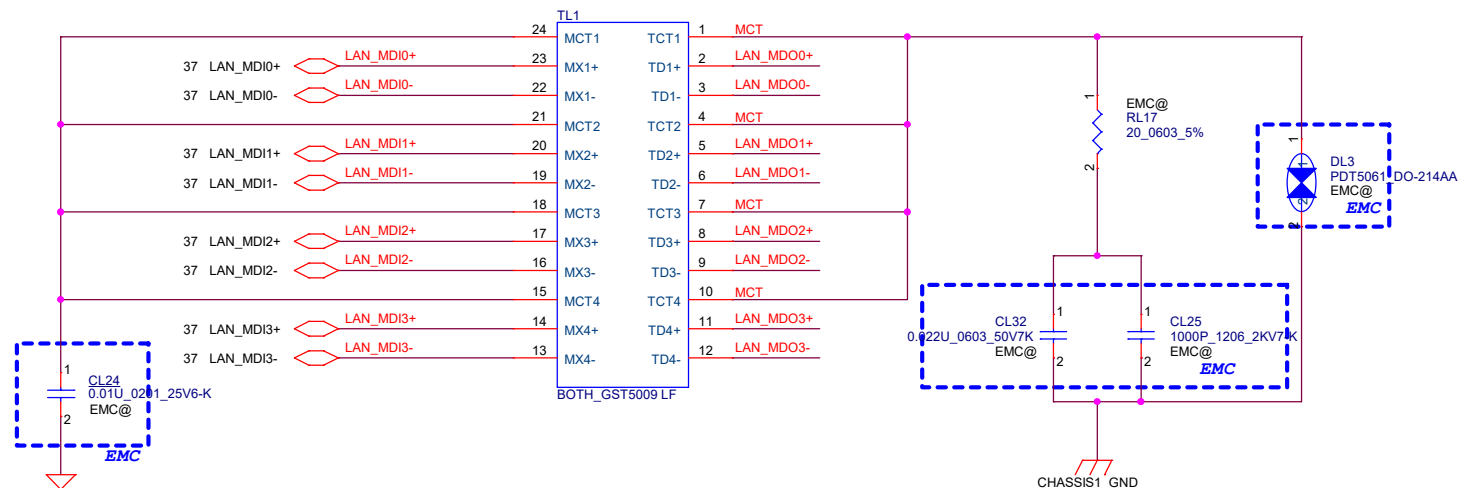
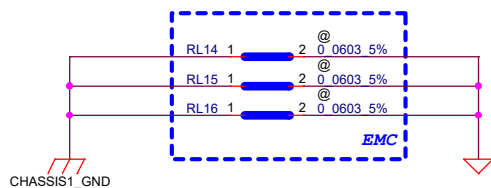
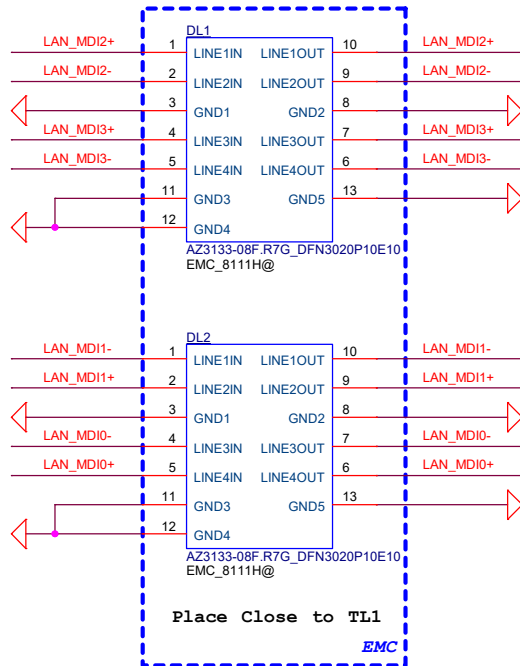
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3				2	Date: Monday, June 26, 2017	Sheet 35 of 60

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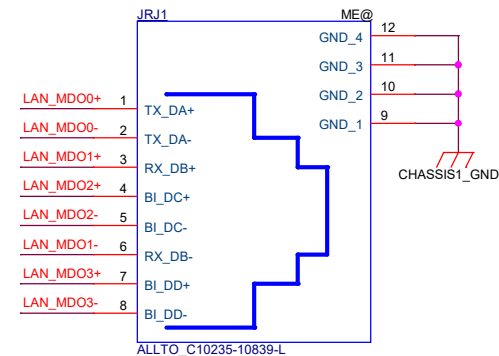
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DL1/DL2
1'S PN:SC300003M00

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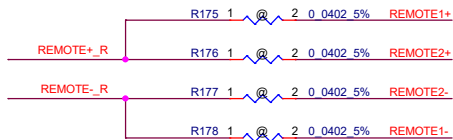
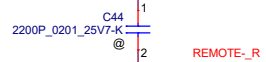
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8/16 Update RJ45 P/N DC021608091 wei

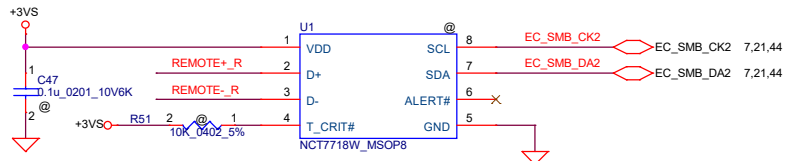
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Close to U1

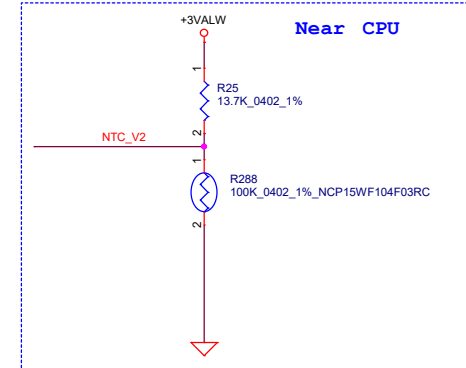
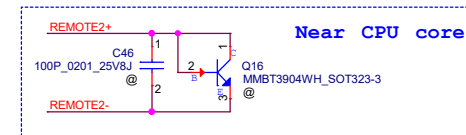
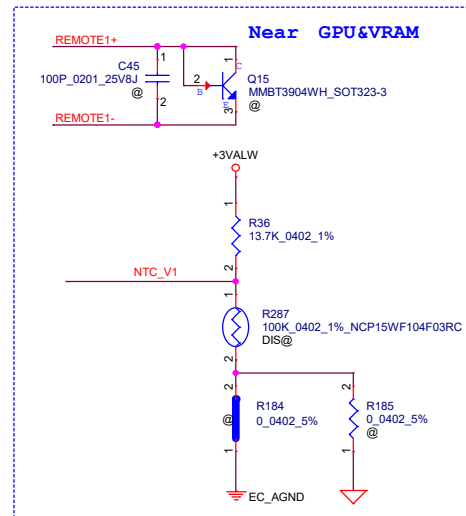


REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

SMSC thermal sensor placed near DIMM

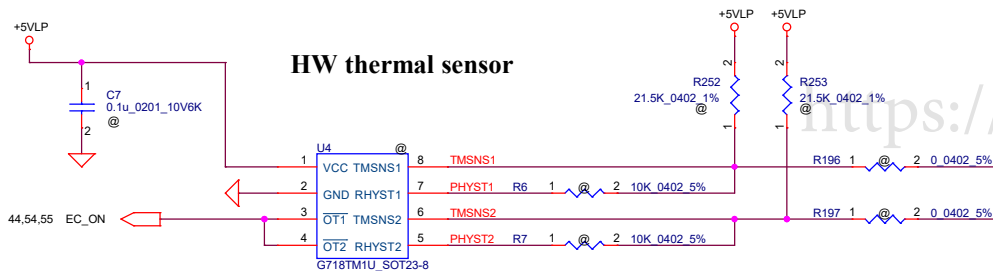


Address 1001_101xb

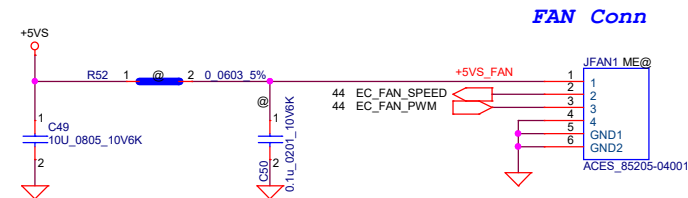


for layout optimized, change the EC_AGND to GND

HW thermal sensor

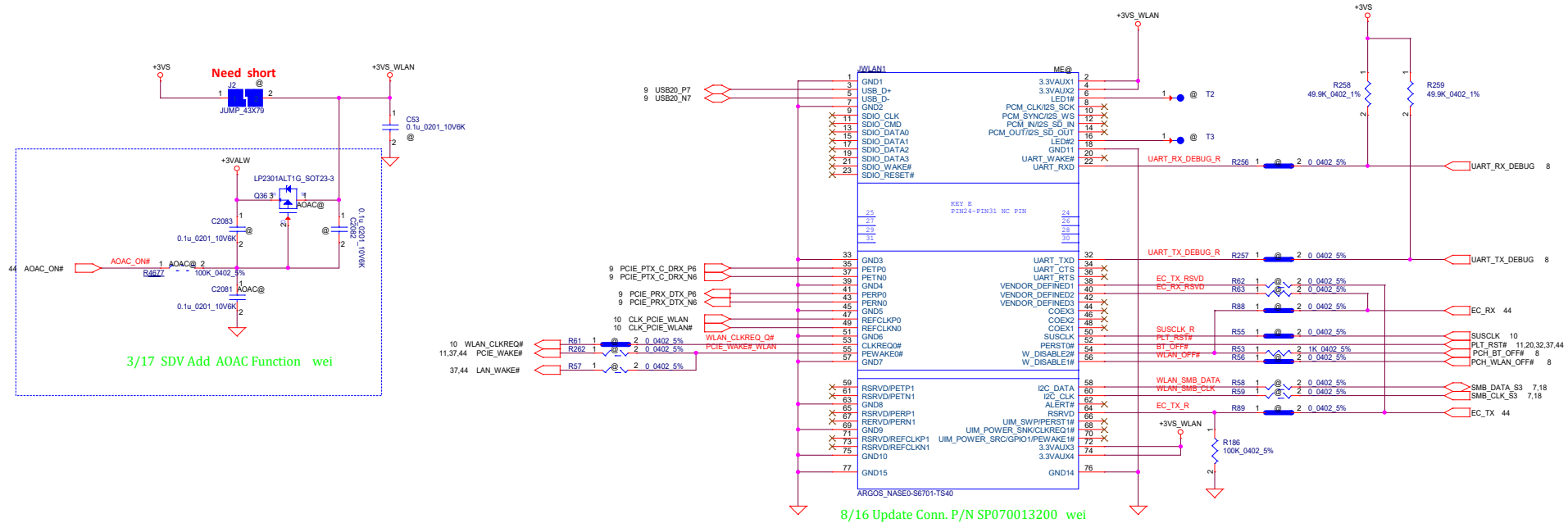


over temperature threshold:
 $RSET = 3 * RTMH$
92+/-30C
Hysteresis temperature threshold.
 $RHYST = (RSET * RTML) / (3 * RTML - RSET)$
56+/-30C



Security Classification	LC Future Center Secret Data			Title	Thermal sensor/FAN Conn	
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Mini-Express Card(WLAN/WiMAX)



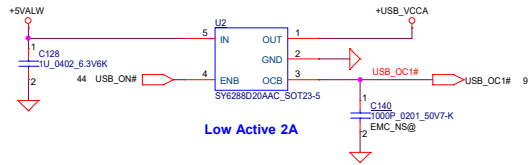
Optane Memory

Optane Memory remove @0913

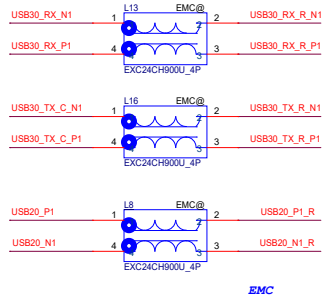
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				Date:	Wednesday, September 13, 2017 1 Sheet 40 of 80

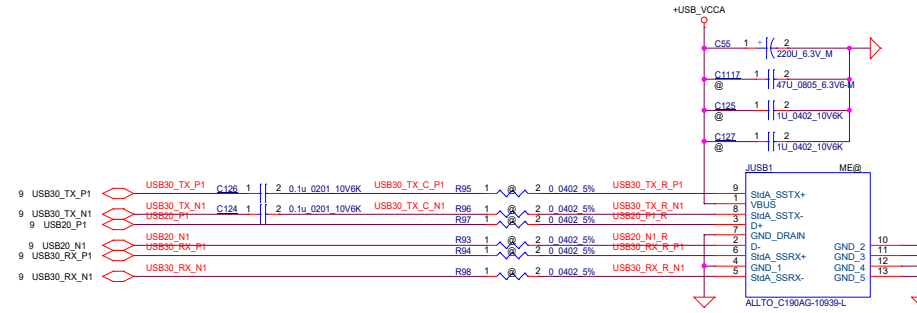
LEFT SIDE USB3.0 PORT x2



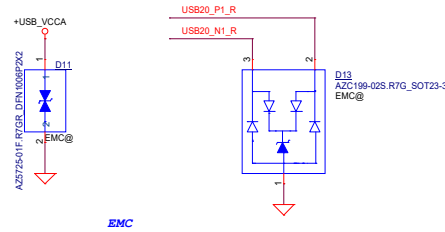
Low Active 2A



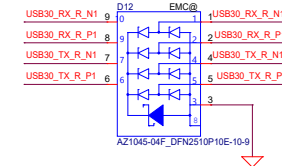
EMC



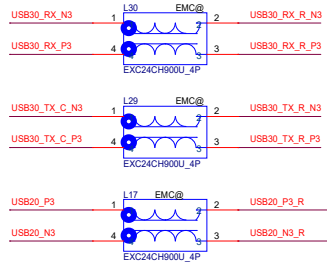
09/05 Update USBConn. P/N DC021609011 wei



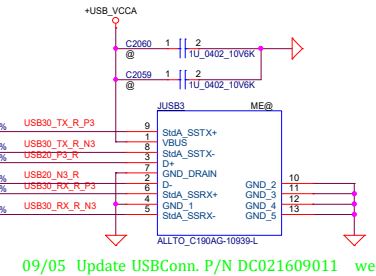
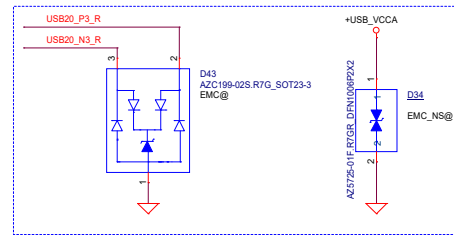
EMC



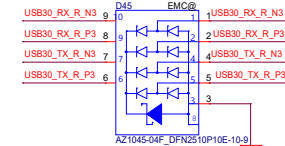
<https://vinafix.com>



FOR ESD Close to Connector

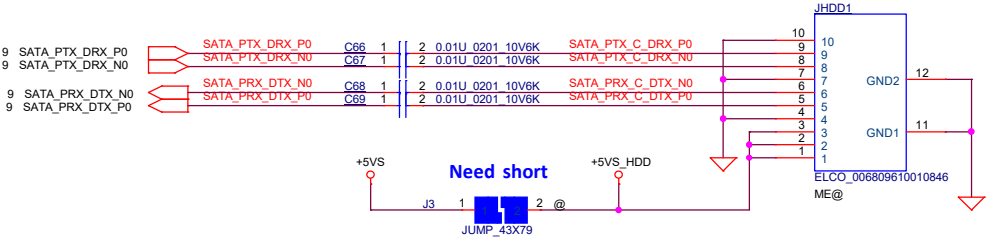
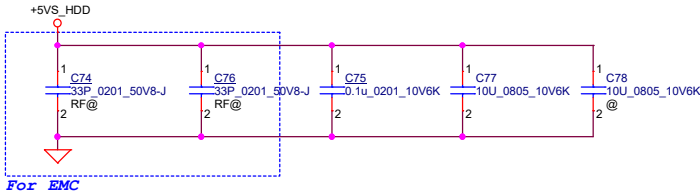


09/05 Update USBConn. P/N DC021609011 wei



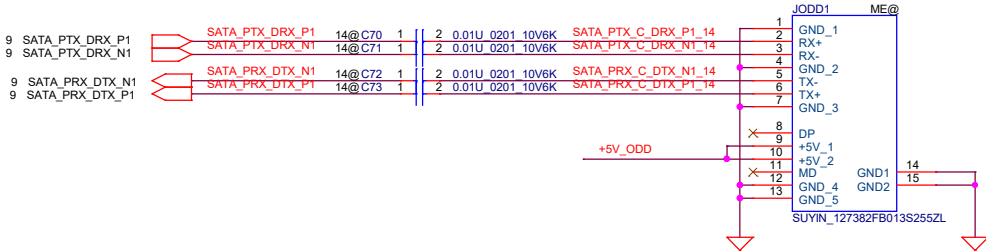
Security Classification	LC Future Center Secret Data		Title	USB3.0 PORT (LEFT)	
Issued Date	2016/12/14	Deciphered Date	2017/12/13	Size	Document Number
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			Date:	Monday, June 28, 2017	Sheet 41 of 80

SATA HDD Conn.

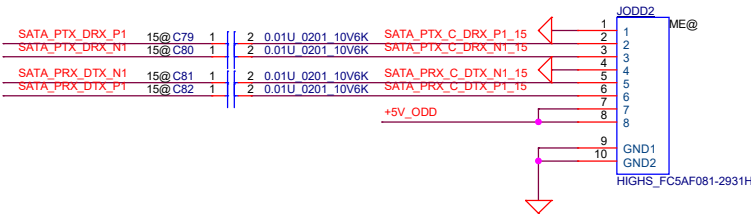


<https://vinafix.com>

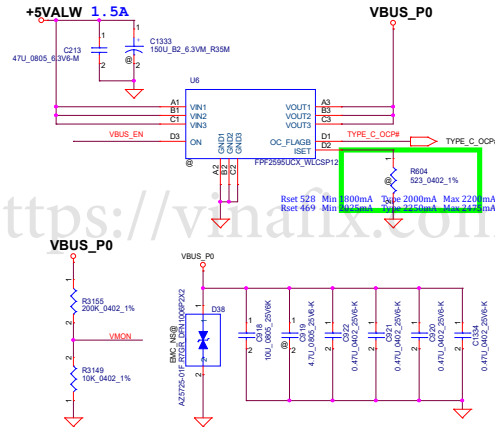
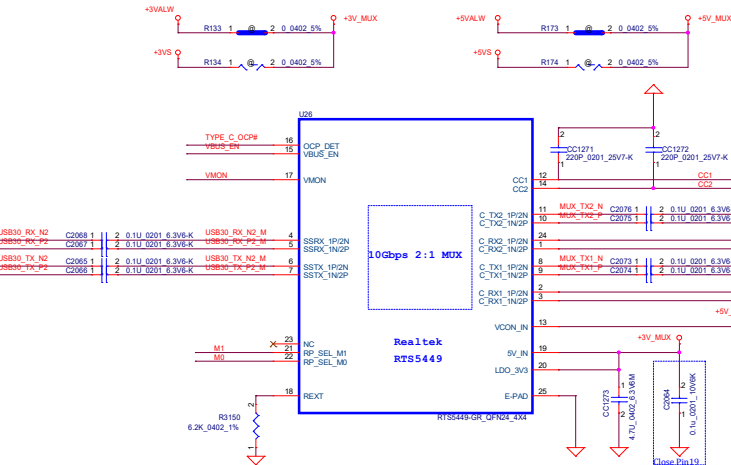
FOR 14" SATA ODD Conn.



FOR 15" 17" SATA ODD FFC Conn



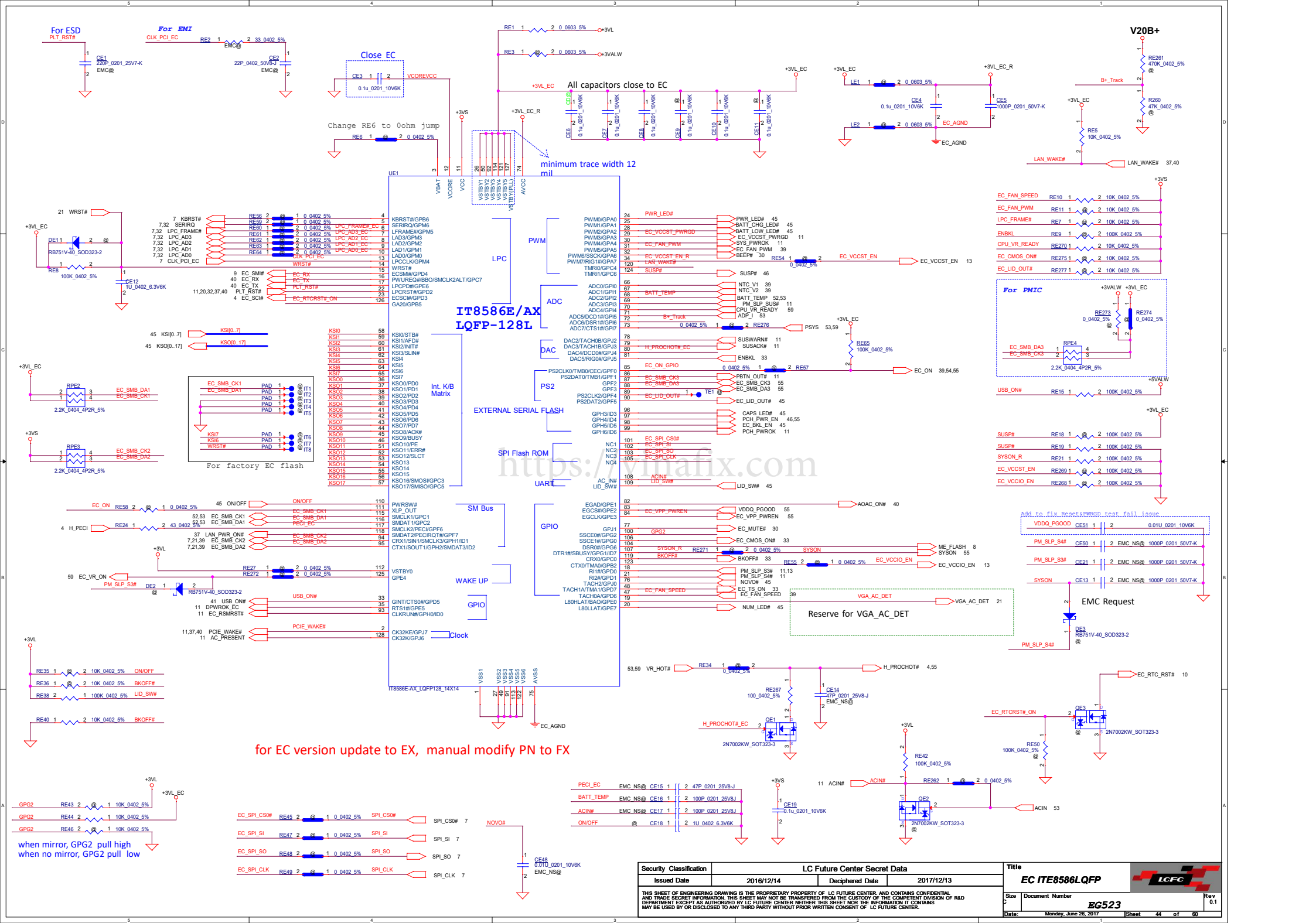
8/16 Update Conn. P/N SP01001YV00 wei



For C_VBUS
power switch OCP pin

Power switch OCP pin	Note
Low Active	R3147 mount
High Active	R3140 mount

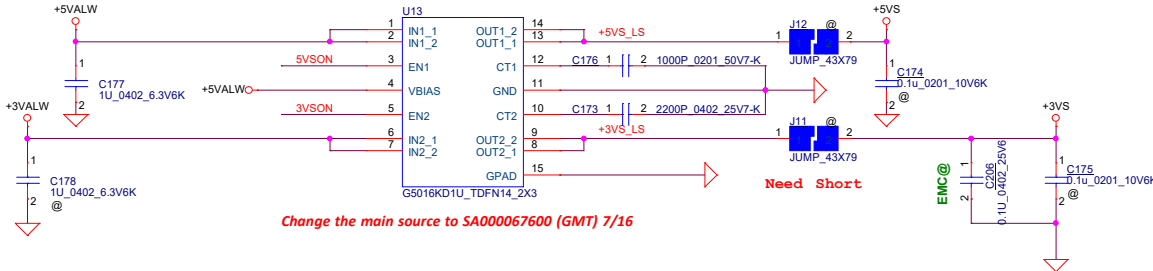
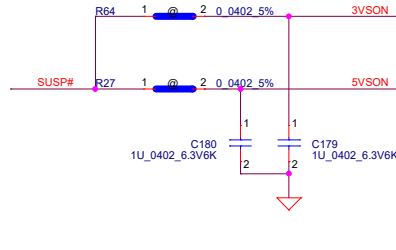




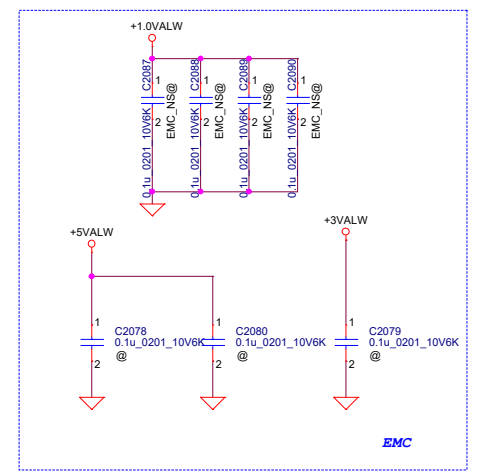
Load Switch
+5VALW To +5VS
+3VALW To +3VS

+3VS, C173 --> 2.74ms
+5VS, C176 --> 2.03ms

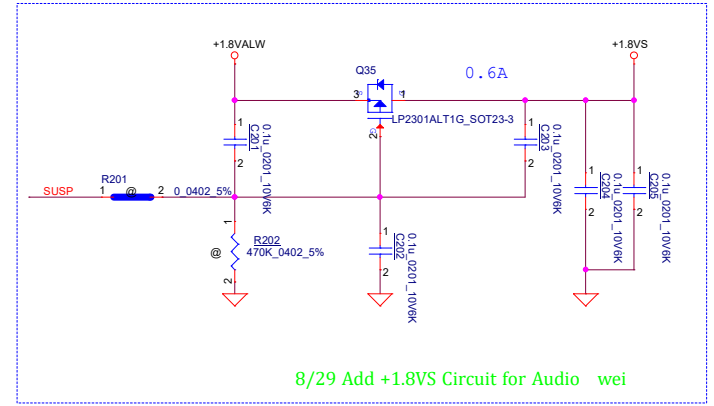
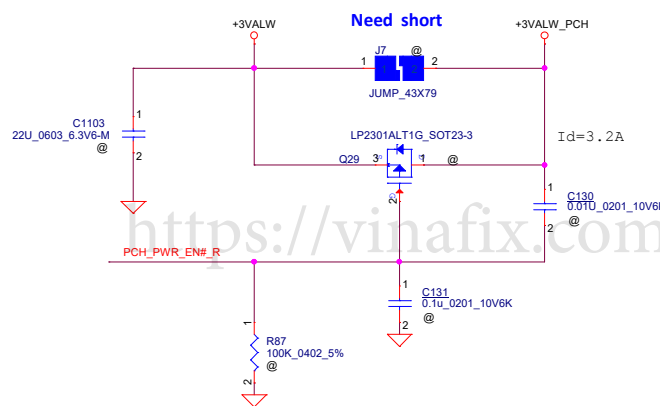
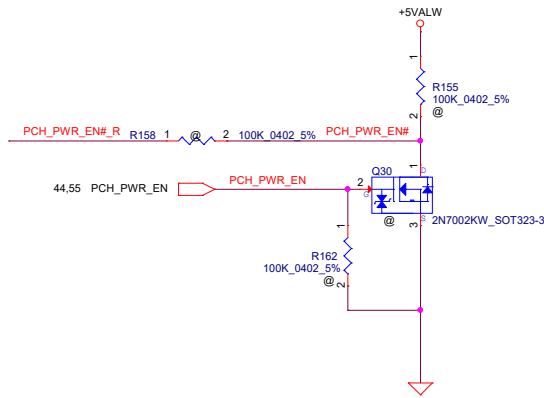
VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm



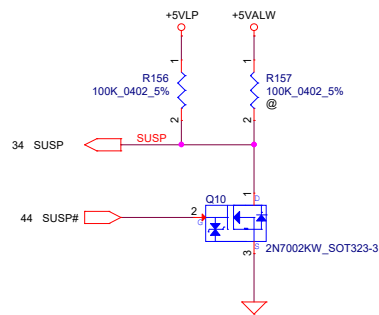
Change the main source to SA000067600 (GMT) 7/16



EMC




8/29 Add +1.8VS Circuit for Audio wei

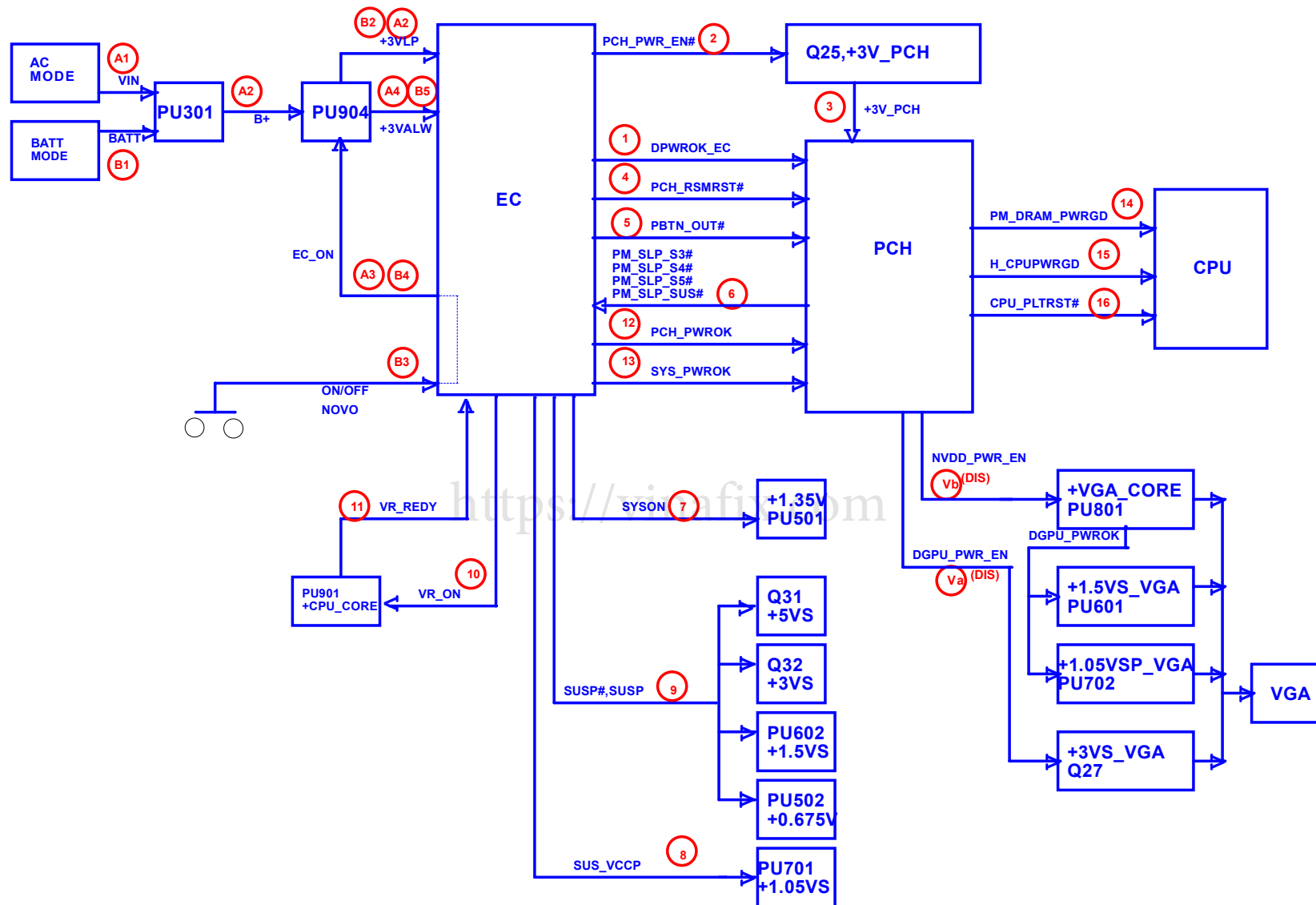


For DisCharge



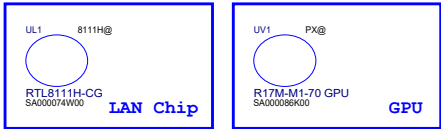
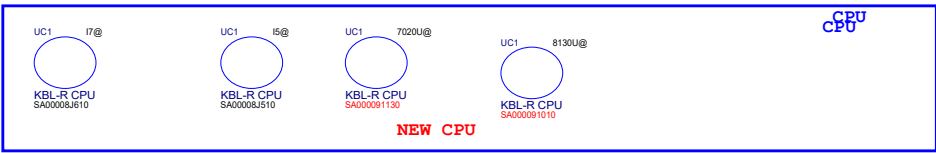
08/29: Need double check enable signal and the resistance

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Size		Document		Number		EG523		Rev	
Custom								0.1	
Date:		Thursday, October 26, 2017		Sheet		46		of 60	

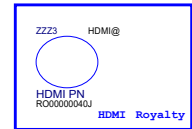
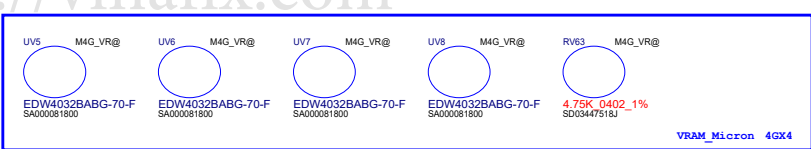
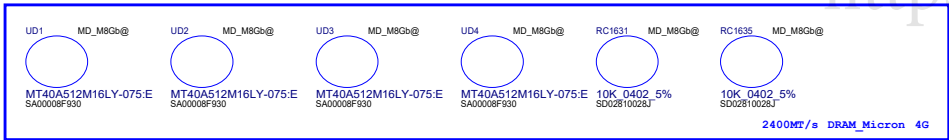
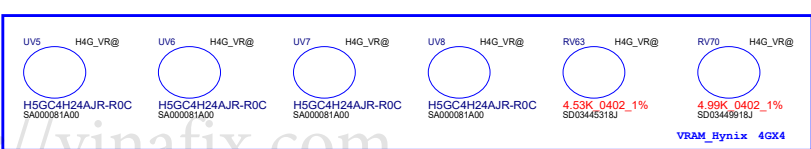
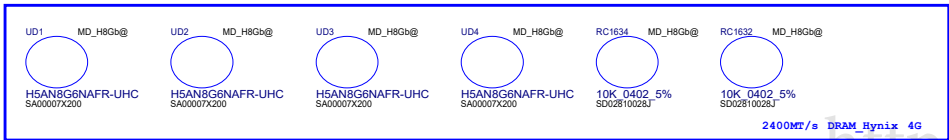
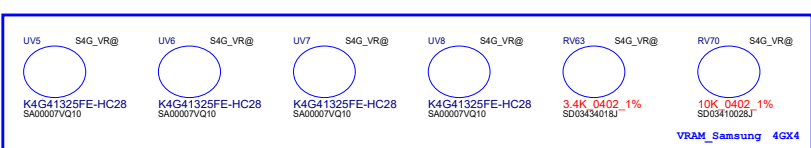
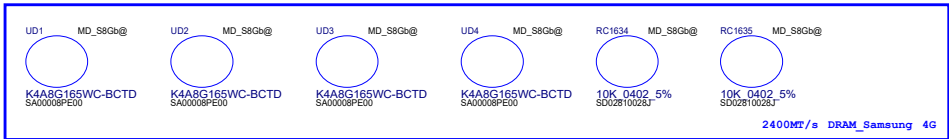
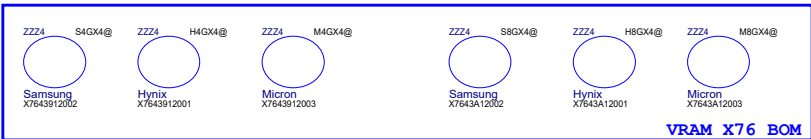
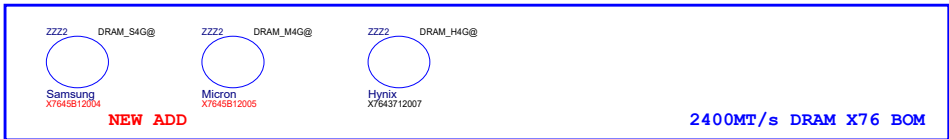


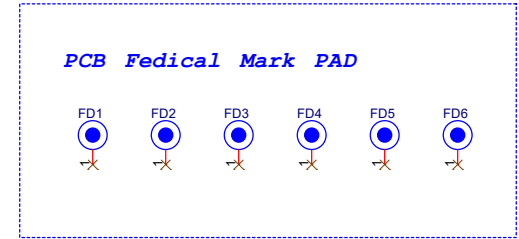
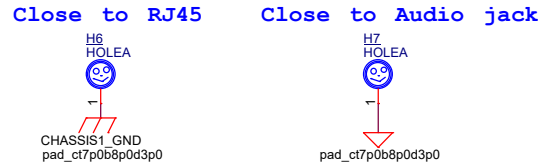
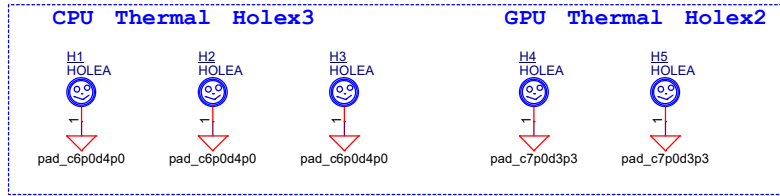
LC Future Center Secret Data			
Security Classification	Issued Date	Deciphered Date	2017/12/13
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Title		Rev	
Power sequence block		0.1	
Size	Document Number	BG523	
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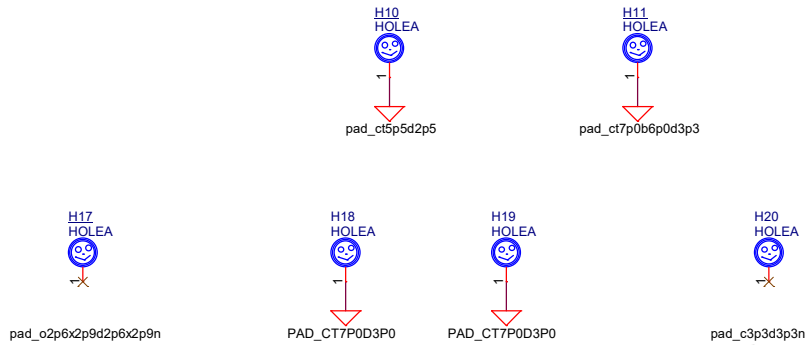
Vinafix.com



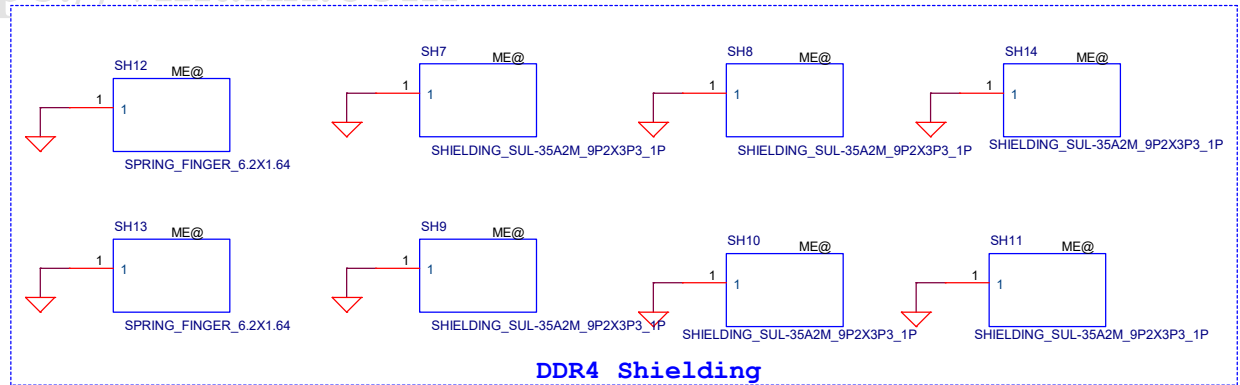
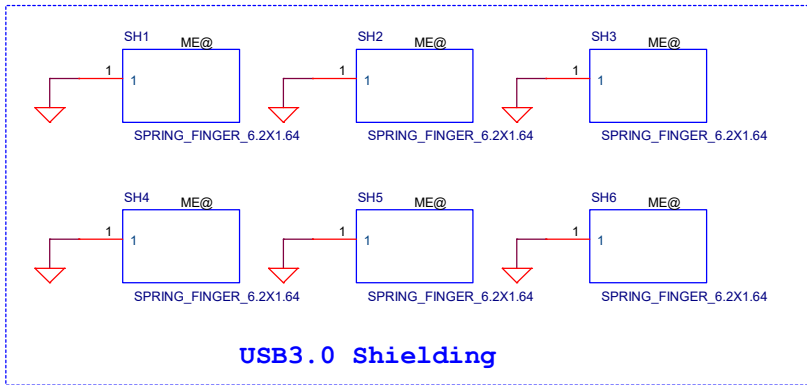


DC-IN x2

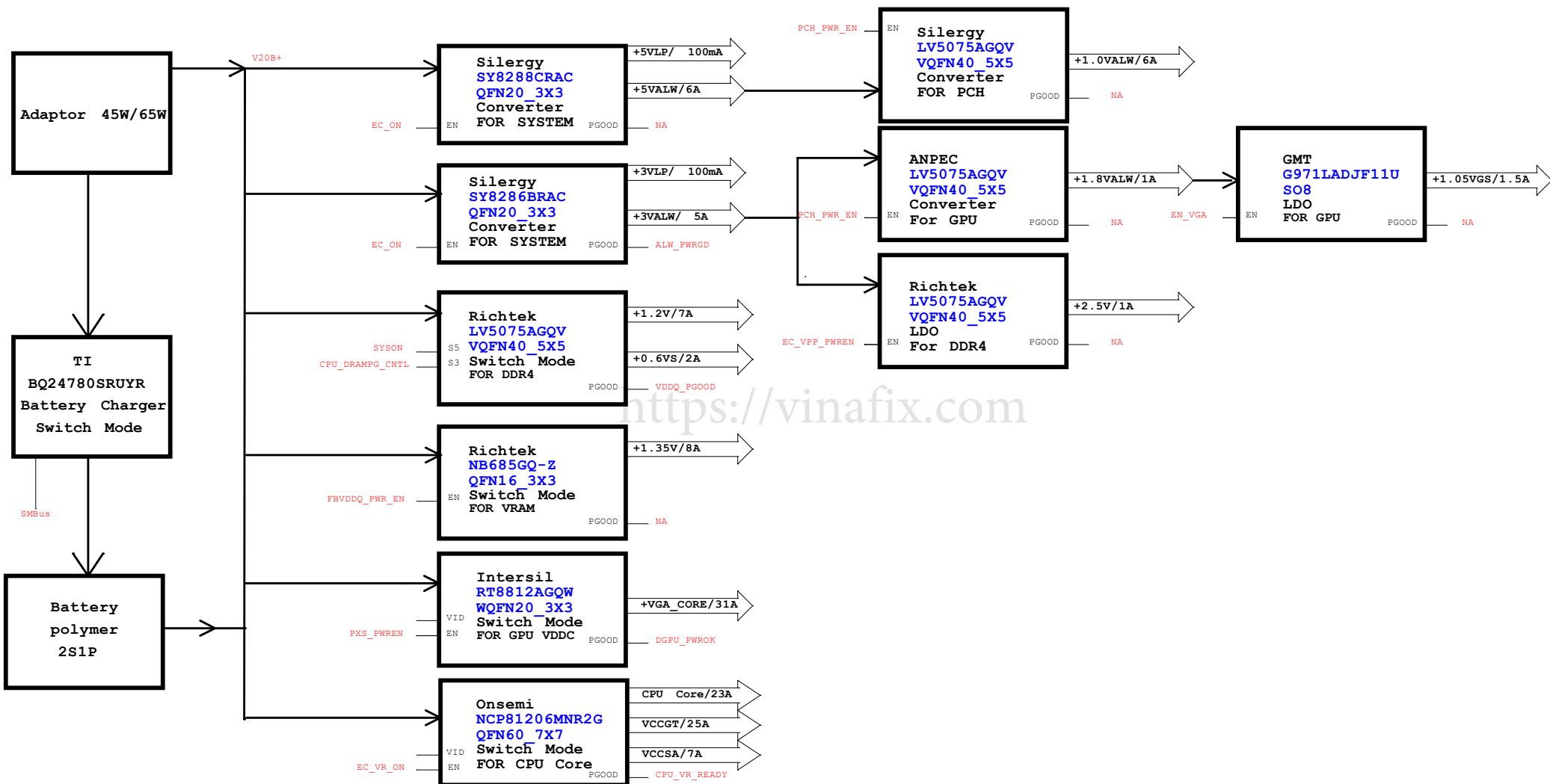
WLAN Standoff

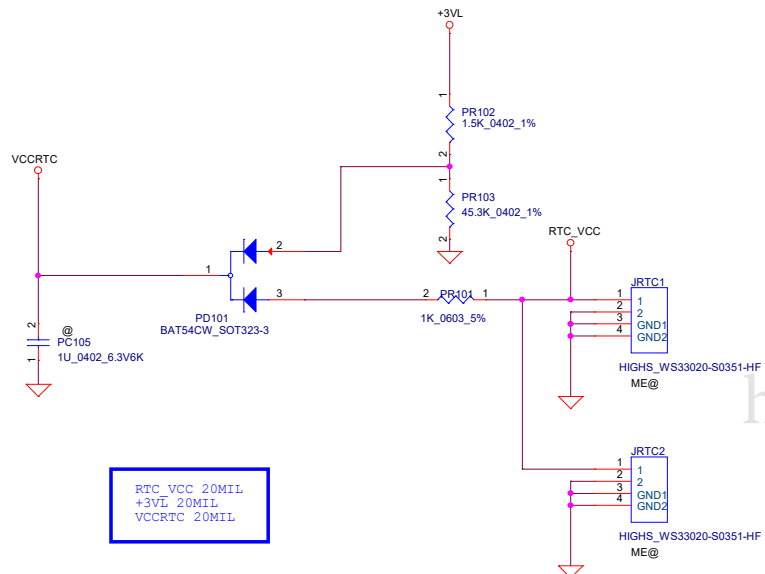
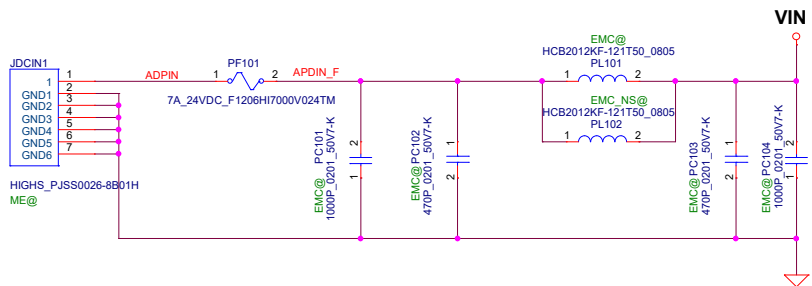


remove H22



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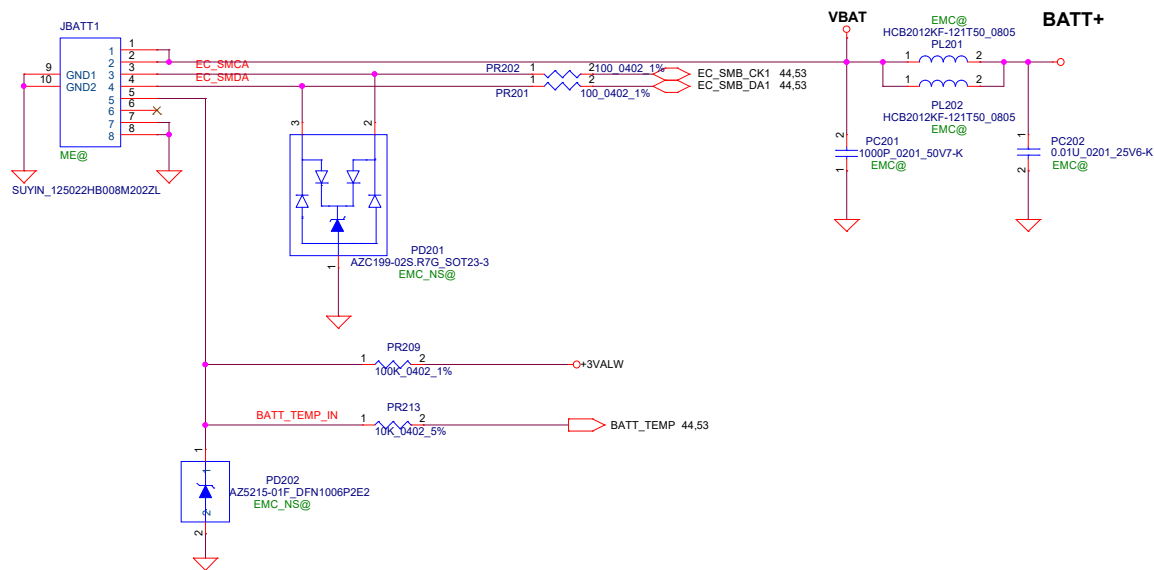
RTC_VCC 20MIL
+3VL 20MIL
VCCRTC 20MIL

No charge RTC with 35mm cable
RTC Battery for GCM BOM
(2nd source and quoted price)

Vinafix.com

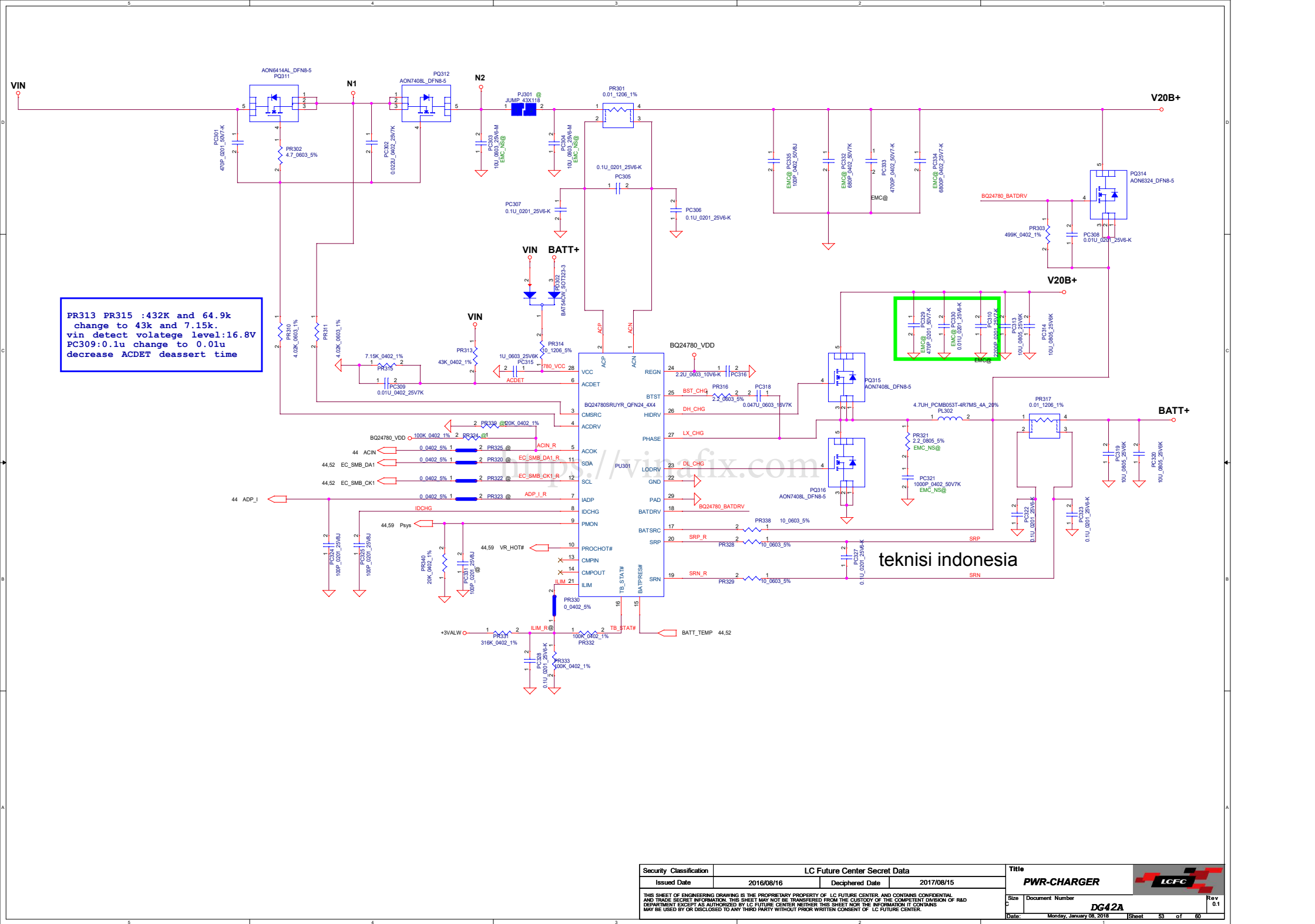
<https://vinafix.com>

Security Classification	LC Future Center Secret Data			Title	PWR-DCIN / RTC charger	
Issued Date	2016/08/16	Deciphered Date	2017/08/15	Size	Document Number	Rev
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2S1P polymer battery
voltage level: +6V ~
8.4 V

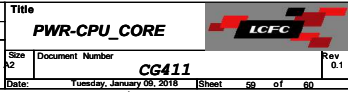
<https://vinafix.com>

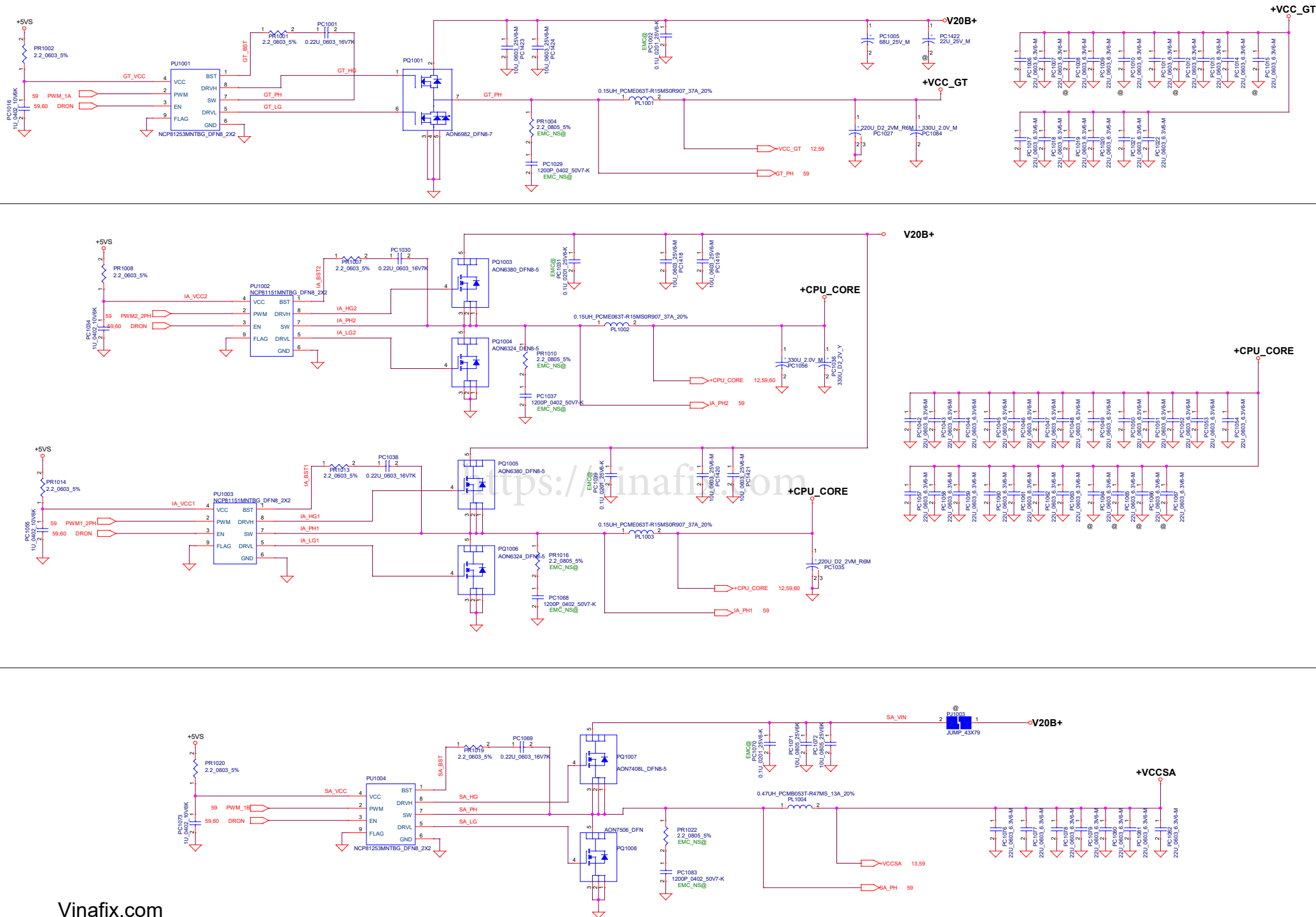


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Security Classification	LC Future Center Secret Data			Title	
Issued Date	2016/08/16	Deciphered Date	2017/08/15	PWR	
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RVboot	Core	GT	SA
35.7K	0V	0V	1.05V





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Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	PWR-CPU_CORE	
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Size	2	Document Number	CG411		Rev. 0.1
Date:	Monday, January 05, 2016	Sheet	60	of	60